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## AT91 Reset Considerations

### Introduction

The AT91 family offers the microprocessor designer a wide variety of architectural features configurable to the user's specific application requirements. These configurations are centered on a register-based core to which may be added on-chip, powerful peripheral components including power management, USART, serial peripheral interface, ADC, DAC, real-time clock and 16-bit multifunctional timers.

The on-chip peripherals may themselves be individually configured to offer a wide variety of functional alternatives. The large number of available options means that the user must specify a number of system parameters by initializing control register contents for the specific peripheral units. The number of registers to be initialized may be considerable for a representative AT91-based system. The objective of this Application Note is to help the user in the initial configuration of the system by describing the AT91 reset state.



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**AT91 ARM<sup>®</sup>  
Thumb<sup>®</sup>  
Microcontrollers**

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**Application  
Note**

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## Reset Sources

Depending on the device, an AT91 microcontroller can have up to two external reset inputs:

- NRST microcontroller reset pin
- NTRST JTAG/ICE reset pin, not available for the AT91x40 Family

Internal reset can also be generated by the watchdog and by software (EBI remap function allows dynamic reset vector). Refer to Table 1.

**Table 1.** Reset Sources

Reset Origin	Reset Cause	Related Signals	Effects
External	Power-up	NRST and NTRST	Power-on reset (cold reset)
	ICE interface	NTRST and/or NRST	ICE reset and/or microcontroller reset
Internal	Watchdog time out	Internal NRST signal or NWDOVF	Internal reset generation or internal Interrupt generation or external NRST activation via NWDOVF
	Software reset	None	Warm reset

NRST is an active low-level input. It is asserted asynchronously but exit from the reset is synchronized internally to the MCK. The signal presented on MCK must be active within the specification for a minimum of 10 clock cycles up to the rising edge of NRST to ensure correct operation.

The watchdog can be programmed to generate an internal reset. In this case, the reset has the same effect as the NRST pin assertion, but the pins BMS and NTRI are not sampled. Boot mode and tri-state mode are not updated. If the NRST pin is asserted and the watchdog triggers the internal reset, the NRST pin has priority.

## Input/Output Considerations

After the reset, the peripheral I/Os are initialized as inputs to provide the user with maximum flexibility. It is recommended that in any application phase, the inputs to the AT91 microcontrollers be held at valid logic levels to minimize the power consumption.

## System Reset

Reset restores the default states of the user interface registers (defined in the user interface of each peripheral), and forces the ARM7TDMI™ to perform the next instruction fetch from address zero. Except for the program counter, the ARM7TDMI registers do not have defined reset states. When reset is active, the inputs of the AT91 microcontrollers must be held at valid logic levels. The External Bus Interface (EBI) address lines drive low during reset.

## Tri-state Mode

The AT91X40 series provides a tri-state mode that is used for debug purposes. This enables the connection of an emulator probe to an application board without having to desolder the device from the target board. In tri-state mode, all the output pin drivers of the AT91X40 series microcontroller are disabled. To enter tri-state mode, the pin NTRI must be held low during the last 10 clock cycles before the rising edge of NRST. For normal operation, the pin NTRI must be held high during reset by a resistor of up to 400K Ohm.

## Boot Sequence

The ARM reset vector is at address 0x0. After the NRST line is released, the ARM7TDMI executes the instruction stored at this address. Thus this address must be mapped to non volatile memory after the reset.

The input level on the BMS pin during the last 10 clock cycles before the rising edge of the NRST selects the type of boot memory. The boot mode depends on the device and whether the AT91 microcontrollers have on-chip ROM or extended SRAM. Refer to Table 2. The user can select either an 8-bit or 16-bit external memory device connected to NCS0 as the boot memory.

**Table 2.** Boot Mode Select

BMS	Product	Boot Memory
1	AT91R40807, AT91FR4081	Internal 32-bit extended SRAM
	AT91M40807	Internal 32-bit ROM
	AT91M40800, AT91R40008, AT91F40816, AT91FR40162, AT91M63200, AT91M43300, AT91M42800A, AT91M55800A	External 8-bit memory on NCS0
0	All AT91 devices	External 16-bit memory on NCS0

## Remap Command

The ARM vectors (Reset, Abort, Data Abort, Prefetch Abort, Undefined Instruction, Interrupt, Fast Interrupt) are mapped from address 0x0 to address 0x20. Refer to Table 3. In order to allow these vectors to be redefined dynamically by the software, the AT91 microcontroller family uses a remap command that enables switching between the boot memory and the internal SRAM bank addresses. The remap command is accessible via the EBI user interface. The remap operation can be changed back only by an internal reset or an NRST assertion.

**Table 3.** ARM Vector Address Mapping

Address	Content
0x00000000	Reset
0x00000004	Undefined Instruction
0x00000008	Software Interrupt
0x0000000C	Prefetch Abort
0x00000010	Data Abort
0x00000014	Reserved
0x00000018	IRQ
0x0000001C	FIQ

## System Peripherals

### External Bus Interface

The EBI generates the signals that control the access to the external memory or peripheral devices. Depending on the device and the BMS pin level during the reset, the user can select either an 8-bit or 16-bit external memory device connected to NCS0 as the boot memory. In this case, EBI\_CSR0 (Chip Select Register 0) is reset at the following configuration for chip select 0:

- 8 wait states (WSE = 1, NWS = 7) for all AT91 devices except the AT91M42800A, 0 wait states (WSE = 0, NWS = 7) for the AT91M42800A.
- 8-bit or 16-bit data bus width, depending on BMS (refer to Table 1)

The EBI provides two alternative protocols for external memory read access: standard and early read. Standard read protocol is the default protocol after reset.

### EBI Configuration/Initialization Registers

Base Address: 0xFFE00000

**Table 4.** External Bus Interface Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Chip Select Register 0	EBI_CSR0	Read/Write	0x0000203E <sup>(1)</sup>	All AT91 devices except AT91M42800A
				0x0000203D <sup>(2)</sup>	All AT91 devices except AT91M42800A
				0x000020E <sup>(1)</sup>	AT91M42800A
				0x000020D <sup>(2)</sup>	AT91M42800A
0x04	Chip Select Register 1	EBI_CSR0	Read/Write	0x10000000	All AT91 devices
0x08	Chip Select Register 2	EBI_CSR0	Read/Write	0x20000000	All AT91 devices
0x0C	Chip Select Register 3	EBI_CSR0	Read/Write	0x30000000	All AT91 devices
0x10	Chip Select Register 4	EBI_CSR0	Read/Write	0x40000000	All AT91 devices
0x14	Chip Select Register 5	EBI_CSR0	Read/Write	0x50000000	All AT91 devices
0x18	Chip Select Register 6	EBI_CSR0	Read/Write	0x60000000	All AT91 devices
0x1C	Chip Select Register 7	EBI_CSR0	Read/Write	0x70000000	All AT91 devices
0x20	Remap Control Register	EBI_RCR	Write only	-	All AT91 devices
0x24	Memory Control Register	EBI_MCR	Read/Write	0	All AT91 devices
0x28	Reserved	-	-	-	AT91M42800A
0x2C	Reserved	-	-	-	AT91M42800A
0x30	Abort Status Register	EBI_ASR	Read only	0	AT91M42800A
0x34	Address Abort Status Register	EBI_AASR	Read only	0	AT91M42800A

Notes: 1. 8-bit boot (if BMS is detected high)  
2. 16-bit boot (if BMS is detected low)

## Power-saving (AT91x40 Family only)

The AT91X40 Series power-saving feature enables optimization of power consumption. The PS controls the CPU and peripheral clocks. The ARM7TDMI clock is enabled after a reset and is automatically re-enabled by any enabled interrupt in the Idle Mode. The peripheral clocks are automatically enabled after a reset.

### PS Configuration/Initialization Registers

Base Address: 0xFFFF4000

**Table 5.** Power-saving Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Control Register	PS_CR	Write only	-	AT91x40 Family
0x04	Peripheral Clock Enable Register	PS_PCER	Write only	-	AT91x40 Family
0x08	Peripheral Clock Disable Register	PS_PCDR	Write only	-	AT91x40 Family
0x0C	Peripheral Clock Status Register	PS_PCSR	Read only	0x17C	AT91x40 Family



**Power Management Controller (AT91M43300, AT91M63200 and AT91M42800A only)**

The Power Management Controller allows optimization of power consumption. The PMC controls the system clocks and the peripherals clocks. It also controls the oscillator and PLLs on the AT91M42800A. The ARM core clock is enabled after a reset and is automatically re-enabled by any enabled interrupt. The peripheral clocks are automatically disabled after a reset.

Note: On the M42800A, after a reset, the CSS field in PMC\_CGMR is 0, selecting the slow clock as source clock.

**PMC Configuration/Initialization Registers**

Base address: 0xFFFF4000

**Table 6.** Power Management Controller Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	System Clock Enable Register	PMC_SCER	Write only	-	AT91M43300, AT91M63200, AT91M42800A
0x04	System Clock Disable Register	PMC_SCDR	Write only	-	AT91M43300, AT91M63200, AT91M42800A
0x08	System Clock Status Register	PMC_SCSR	Read only	0x1	AT91M43300, AT91M63200, AT91M42800A
0x0C	Reserved	-	-	-	AT91M43300, AT91M63200, AT91M42800A
0x10	Peripheral Clock Enable Register	PMC_PCER	Write only	-	AT91M43300, AT91M63200, AT91M42800A
0x14	Peripheral Clock Disable Register	PMC_PCDR	Write only	-	AT91M43300, AT91M63200, AT91M42800A
0x18	Peripheral Clock Status Register	PMC_PCSR	Read only	0	AT91M43300, AT91M63200, AT91M42800A
0x1C	Reserved	-	-	-	AT91M43300, AT91M63200, AT91M42800A
0x20	Clock Generator Mode Register	PMC_CGMR	Read/write	0	AT91M43300, AT91M63200, AT91M42800A
0x24	Reserved	-	-	-	AT91M43300, AT91M63200, AT91M42800A
0x28	Reserved	-	-	-	AT91M43300, AT91M63200, AT91M42800A
0x2C	Reserved	-	-	-	AT91M43300, AT91M63200, AT91M42800A
0x30	Status Register	PMC_SR	Read only	0	AT91M43300, AT91M63200, AT91M42800A
0x34	Interrupt Enable Register	PMC_IER	Write only	-	AT91M43300, AT91M63200, AT91M42800A
0x38	Interrupt Disable Register	PMC_IDR	Write only	-	AT91M43300, AT91M63200, AT91M42800A
0x3C	Interrupt Mask Register	PMC_IMR	Read only	0	AT91M43300, AT91M63200, AT91M42800A

## Advanced Power Management Controller (AT91M55800A only)

The Advanced Power Management Controller optimizes the power consumption of the device and the complete system. The APMC controls the clocking elements such as the oscillators and the PLL, the core and the peripheral clocks, and has the capability to control the system power supply.

The ARM Core clock is enabled after a reset and is automatically re-enabled by any enabled interrupt. The peripheral clocks are automatically disabled after a reset. At reset, the source of MCK is the slow clock (32768 Hz) to minimize the power required to start up the system, the main oscillator is disabled.

### APMC Configuration/Initialization Registers

Base Address: 0xFFFF4000

**Table 7.** Advanced Power Management Controller Registers

Offset	Register	Name	Access	Main Reset	Backup Reset	Product
0x00	System Clock Enable Register	APMC_SCER	Write only	-	-	AT91M55800A
0x04	System Clock Disable Register	APMC_SCDR	Write only	-	-	AT91M55800A
0x08	System Clock Status Register	APMC_SCSR	Read only	0x1	-	AT91M55800A
0x0C	Reserved	-	-	-	-	AT91M55800A
0x10	Peripheral Clock Enable Register	APMC_PCER	Write only	-	-	AT91M55800A
0x14	Peripheral Clock Disable Register	APMC_PCDR	Write only	-	-	AT91M55800A
0x18	Peripheral Clock Status Register	APMC_PCSR	Read only	0	-	AT91M55800A
0x1C	Reserved	-	-	-	-	AT91M55800A
0x20	Clock Generator Mode Register	APMC_CGMR	Read/write	0	-	AT91M55800A
0x24	Reserved	-	-	-	-	AT91M55800A
0x28	Power Control Register	APMC_PCR	Write only	-	-	AT91M55800A
0x2C	Power Mode Register	APMC_PMR	Read/Write	-	0x1	AT91M55800A
0x30	Status Register	APMC_SR	Read only	0	-	AT91M55800A
0x34	Interrupt Enable Register	APMC_IER	Write only	-	-	AT91M55800A
0x38	Interrupt Disable Register	APMC_IDR	Write only	-	-	AT91M55800A
0x3C	Interrupt Mask Register	APMC_IMR	Read only	0	-	AT91M55800A



## Advanced Interrupt Controller

The Advanced Interrupt Controller has 8-level priority, individually maskable, vectored. This feature substantially reduces the software and real-time overhead in handling internal and external interrupts.

After a hardware reset, the AIC pins are controlled by the PIO Controller. They must be configured to be controlled by the peripheral before being used.

### AIC Configuration/Initialization Registers

Base Address: 0xFFFFF000

**Table 8.** Advanced Interrupt Controller Registers

Offset	Register	Name	Access	Reset Value	Product
0x000	Source Mode Register 0	AIC_SMR0	Read/Write	0	All AT91 devices
0x004	Source Mode Register 1	AIC_SMR1	Read/Write	0	All AT91 devices
-	-	-	Read/Write	0	All AT91 devices
0x07C	Source Mode Register 31	AIC_SMR31	Read/Write	0	All AT91 devices
0x080	Source Vector Register 0	AIC_SVR0	Read/Write	0	All AT91 devices
0x084	Source Vector Register 1	AIC_SVR1	Read/Write	0	All AT91 devices
-	-	-	Read/Write	0	All AT91 devices
0x0FC	Source Vector Register 31	AIC_SVR31	Read/Write	0	All AT91 devices
0x100	IRQ Vector Register	AIC_IVR	Read only	0	All AT91 devices
0x104	FIQ Vector Register	AIC_FVR	Read only	0	All AT91 devices
0x108	Interrupt Status Register	AIC_ISR	Read only	0	All AT91 devices
0x10C	Interrupt Pending Register	AIC_IPR	Read only	(see Note)	All AT91 devices
0x110	Interrupt Mask Register	AIC_IMR	Read only	0	All AT91 devices
0x114	Core Interrupt Status Register	AIC_CISR	Read only	0	All AT91 devices
0x118	Reserved	-	-	-	All AT91 devices
0x11C	Reserved	-	-	-	All AT91 devices
0x120	Interrupt Enable Command Register	AIC_IECR	Write only	-	All AT91 devices
0x124	Interrupt Disable Command Register	AIC_IDCR	Write only	-	All AT91 devices
0x128	Interrupt Clear Command Register	AIC_ICCR	Write only	-	All AT91 devices
0x12C	Interrupt Set Command Register	AIC_ISCR	Write only	-	All AT91 devices
0x130	End of Interrupt Command Register	AIC_EOICR	Write only	-	All AT91 devices
0x134	Spurious Vector Register	AIC_SPU	Read/Write	0	All AT91 devices

Note: The reset value of this register depends on the level of the external IRQ lines. All other sources are cleared at reset.

## Peripheral Input/Output Controller

Depending on the device, the AT91 microcontrollers can have up to a maximum of 58 programmable lines dedicated to input/output. Some I/O lines are dedicated as general-purpose I/O pins. The other I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. The PIO controller enables the generation of an interrupt on an input change and the insertion of a simple input glitch filter on any of the PIO pins.

After reset, the pin is generally controlled by the PIO Controller and is in input mode.

### PIO Configuration/Initialization Registers:

PIO Base Address: 0xFFFF0000 (AT91x40 Family)

PIO Controller A Base Address: 0xFFFE0000 (All AT91 except AT91x40 Family)

PIO Controller B Base Address: 0xFFFF0000 (All AT91 except AT91x40 Family)

**Table 9.** Peripheral Input/Output Controller Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	PIO Enable Register	PIO_PER	Write only	-	All AT91 devices
0x04	PIO Disable Register	PIO_PDR	Write only	-	All AT91 devices
0x08	PIO Status Register	PIO_PSR	Read only	0x01FFFFFF	AT91x40 Family
				0x3FFFFFFF(A)	AT91M55800A, AT91M63200, AT91M43300
				0x0FFFFFFF(B)	AT91M55800A, AT91M63200, AT91M43300
				0x3DFFFFFF(A)	AT91M42800A
				0x00FFFC0(B)	AT91M42800A
0x0C	Reserved	-	-	-	All AT91 devices
0x10	Output Enable Register	PIO_OER	Write only	-	All AT91 devices
0x14	Output Disable Register	PIO_ODR	Write only	-	All AT91 devices
0x18	Output Status Register	PIO_OSR	Read only	0	All AT91 devices
0x1C	Reserved	-	-	-	All AT91 devices
0x20	Input Filter Enable Register	PIO_IFER	Write only	-	All AT91 devices
0x24	Input Filter Disable Register	PIO_IFDR	Write only	-	All AT91 devices
0x28	Input Filter Status Register	PIO_IFSR	Read only	0	All AT91 devices
0x2C	Reserved	-	-	-	All AT91 devices
0x30	Set Output Data Register	PIO_SODR	Write only	-	All AT91 devices
0x34	Clear Output Data Register	PIO_CODR	Write only	-	All AT91 devices
0x38	Output Data Status Register	PIO_ODSR	Read only	0	All AT91 devices
0x3C	Pin Data Status Register	PIO_PDSR	Read only	(see Note 1)	All AT91 devices
0x40	Interrupt Enable Register	PIO_IER	Write only	-	All AT91 devices
0x44	Interrupt Disable Register	PIO_IDR	Write only	-	All AT91 devices
0x48	Interrupt Mask Register	PIO_IMR	Read only	0	All AT91 devices
0x4C	Interrupt Status Register	PIO_ISR	Read only	(see Note 2)	All AT91 devices

**Table 9.** Peripheral Input/Output Controller Registers (Continued)

Offset	Register	Name	Access	Reset Value	Product
0x50	Multi-driver Enable Register	PIO_MDER	Write only	-	All AT91 devices except AT91x40 Family
0x54	Multi-driver Disable Register	PIO_MDDR	Write only	-	All AT91 devices except AT91x40 Family
0x58	Multi-driver Status Register	PIO_MDSR	Read only	0	All AT91 devices except AT91x40 Family
0x5C	Reserved	-	-	-	All AT91 devices except AT91x40 Family

- Notes:
1. The reset value of this register depends on the level of the external pins at reset.
  2. This register is cleared at reset. However, the first read of this register can give a value not equal to zero if any changes have occurred on any pins between the reset and the read.

## Watchdog Timer

The Watchdog Timer can be used to prevent system lock-up if the software becomes trapped in a deadlock.

### Watchdog Timer Configuration/Initialization Registers

Base Address: 0xFFFF8000

**Table 10.** Watchdog Timer Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Overflow Mode Register	WD_OMR	Read/Write	0	All AT91 except AT91M42800A
0x04	Clock Mode Register	WD_CMR	Read/Write	0	All AT91 except AT91M42800A
0x08	Control Register	WD_CR	Write only	-	All AT91 except AT91M42800A
0x0C	Status Register	WD_SR	Read only	0	All AT91 except AT91M42800A

## System Timer (AT91M42800A only)

The System Timer module integrates three different free-running timers:

- A Period Interval Timer setting the base time for an Operating System.
- A Watchdog Timer having capabilities to reset the system in case of software deadlock.
- A Real-time Timer counting elapsed seconds.

These timers count using the Slow Clock. Typically, this clock has a frequency of 32.768 kHz.

### System Timer Configuration/Initialization Registers

Base Address: 0xFFFF8000

**Table 11.** System Timer Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Control Register	ST_CR	Write only	-	AT91M42800A
0x04	Period Interval Mode Register	ST_PIMR	Read/Write	0 <sup>(1)</sup>	AT91M42800A
0x08	Watchdog Mode Register	ST_WDMR	Read/Write	0x00020000 <sup>(1)</sup>	AT91M42800A
0x0C	Real-time Mode Register	ST_RTMR	Read/Write	0x00008000	AT91M42800A
0x10	Status Register	ST_SR	Read only	-	AT91M42800A
0x14	Interrupt Enable Register	ST_IER	Write only	-	AT91M42800A
0x18	Interrupt Disable Register	ST_IDR	Write only	-	AT91M42800A
0x1C	Interrupt Mask Register	ST_IMR	Read only	0	AT91M42800A
0x20	Real-time Alarm Register	ST_RTAR	Read/Write	0	AT91M42800A
0x24	Current Real-time Register	ST_CRTR	Read only	0	AT91M42800A

Note: 1. Corresponds to maximum value of the counter.

## Special Function

The Special Function module integrates the Chip ID, the Reset Status and the Protect registers.

### Special Function Configuration/Initialization Registers

Base Address: 0xFFFF0000

**Table 12.** Special Function Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Chip ID Register	SF_CIDR	Read only	Hardwired	All AT91 devices
0x04	Chip ID Extension Register	SF_EXID	Read only	Hardwired	All AT91 devices
0x08	Reset Status Register	SF_RSR	Read only		All AT91 devices
0x0C	Memory Mode Register	SF_MMR	Read/Write	0x0	AT91x40 Family
	Reserved	-	-	-	All AT91 devices except AT91x40
0x10	Reserved	-	-	-	All AT91 devices
0x14	Reserved	-	-	-	All AT91 devices
0x18	Protect Mode Register	SF_PMR	Read/Write	0x0	All AT91 devices

## User Peripherals

### Universal Synchronous/ Asynchronous Receiver/Transmitter

After a hardware reset, the USART pins are not enabled by default. The user must configure the PIO Controller before enabling the transmitter or receiver. See “Peripheral Input/Output Controller” on page 9 for details.

#### USART Configuration/Initialization Registers:

Base Address USART0: 0xFFFC0000

Base Address USART1: 0xFFFC4000

Base Address USART2: 0xFFFC8000 (AT91M43300, AT91M63200 and AT91M55800A)

**Table 13.** USART Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Control Register	US_CR	Write only	-	All AT91 devices
0x04	Mode Register	US_MR	Read/Write	0	All AT91 devices
0x08	Interrupt Enable Register	US_IER	Write only	-	All AT91 devices
0x0C	Interrupt Disable Register	US_IDR	Write only	-	All AT91 devices
0x10	Interrupt Mask Register	US_IMR	Read only	0	All AT91 devices
0x14	Channel Status Register	US_CSR	Read only	0x18	All AT91 devices
0x18	Receiver Holding Register	US_RHR	Read only	0	All AT91 devices
0x1C	Transmitter Holding Register	US_THR	Write only	-	All AT91 devices
0x20	Baud Rate Generator Register	US_BRGR	Read/Write	0	All AT91 devices
0x24	Receiver Time-out Register	US_RTOR	Read/Write	0	All AT91 devices
0x28	Transmitter Time-guard Register	US_TTGR	Read/Write	0	All AT91 devices
0x2C	Reserved	-	-	-	All AT91 devices
0x30	Receive Pointer Register	US_RPR	Read/Write	0	All AT91 devices
0x34	Receive Counter Register	US_RCR	Read/Write	0	All AT91 devices
0x38	Transmit Pointer Register	US_TPR	Read/Write	0	All AT91 devices
0x3C	Transmit Counter Register	US_TCR	Read/Write	0	All AT91 devices

## Timer/Counter

After a hardware reset, the Timer Counter block pins are controlled by the PIO. They must be controlled by the peripheral before being used.

### TC Configuration/Initialization Registers

TC Base Address: 0xFFFE0000 (AT91x40 Family)

TC Block 0 Base Address: 0xFFFD0000 (All AT91 except AT91x40 Family)

TC Block 1 Base Address: 0xFFFD4000 (All AT91 except AT91x40 Family)

**Table 14.** Timer/Counter Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Channel Control Register	TC_CCR	Write only	-	All AT91 devices
0x04	Channel Mode Register	TC_CMR	Read/Write	0	All AT91 devices
0x08	Reserved	-	-	-	All AT91 devices
0x0C	Reserved	-	-	-	All AT91 devices
0x10	Counter Value	TC_CV	Read/Write	0	All AT91 devices
0x14	Register A	TC_RA	Read/Write <sup>(1)</sup>	0	All AT91 devices
0x18	Register B	TC_RB	Read/Write <sup>(1)</sup>	0	All AT91 devices
0x1C	Register C	TC_RC	Read/Write	0	All AT91 devices
0x20	Status Register	TC_SR	Read only	-	All AT91 devices
0x24	Interrupt Enable Register	TC_IER	Write only	-	All AT91 devices
0x28	Interrupt Disable Register	TC_IDR	Write only	-	All AT91 devices
0x2C	Interrupt Mask Register	TC_IMR	Read only	0	All AT91 devices

Note: 1. Read-only if WAVE = 0.

## Serial Peripheral Interface (AT91M63200, AT91M43300, AT91M42800A and AT91M55800A only)

After a hardware reset, the SPI clock is disabled by default. The user must configure the Power Management Controller (AT91M63200, AT91M43300 and AT91M42800A) or the Advanced Power Management Controller (AT91M55800A) before any access to the user interface of the SPI.

After a hardware reset, the SPI pins are deselected by default. The user must configure the PIO controller to enable the corresponding pins for their SPI functions.

### SPI Configuration/Initialization Registers

Base Address: 0xFFFBC000 (AT91M43300, AT91M63200 and AT91M55800A)

SPIA Base Address: 0xFFFC8000 (AT91M42800A)

SPIB Base Address: 0xFFFC0000 (AT91M42800A)

**Table 15.** Serial Peripheral Interface Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Control Register	SP_CR	Write only	-	All AT91 except AT91x40
0x04	Mode Register	SP_MR	Read/Write	0	All AT91 except AT91x40
0x08	Receive Data Register	SP_RDR	Read only	0	All AT91 except AT91x40
0x0C	Transmit Data Register	SP_TDR	Write only	-	All AT91 except AT91x40
0x10	Status Register	SP_SR	Read only	0	All AT91 except AT91x40
0x14	Interrupt Enable Register	SP_IER	Write only	-	All AT91 except AT91x40
0x18	Interrupt Disable Register	SP_IDR	Write only	-	All AT91 except AT91x40
0x1C	Interrupt Mask Register	SP_IMR	Read only	0	All AT91 except AT91x40
0x20	Receive Pointer Register	SP_RPR	Read/Write	0	All AT91 except AT91x40
0x24	Receive Counter Register	SP_RCR	Read/Write	0	All AT91 except AT91x40
0x28	Transmit Pointer Register	SP_TPR	Read/Write	0	All AT91 except AT91x40
0x2C	Transmit Counter Register	SP_TCR	Read/Write	0	All AT91 except AT91x40
0x30	Chip Select Register 0	SP_CSR0	Read/Write	0	All AT91 except AT91x40
0x34	Chip Select Register 1	SP_CSR1	Read/Write	0	All AT91 except AT91x40
0x38	Chip Select Register 2	SP_CSR2	Read/Write	0	All AT91 except AT91x40
0x3C	Chip Select Register 3	SP_CSR3	Read/Write	0	All AT91 except AT91x40



## Analog-to-digital Converter (AT91M55800A only)

Two identical 4-channel 10-bit analog-to-digital converters (ADC) based on a Successive Approximation Register (SAR) approach. By default after a reset, the ADC operates in 10-bit mode.

### ADC Configuration/Initialization Registers

Base Address ADC 0: 0xFFFFB0000

Base Address ADC 1: 0xFFFFB4000

**Table 16.** ADC Registers

Offset	Register	Name	Access	Reset Value	Product
0x00	Control Register	ADC_CR	Write only	-	AT91M55800A
0x04	Mode Register	ADC_MR	Read/Write	0	AT91M55800A
0x08	Reserved	-	-	-	AT91M55800A
0x0C	Reserved	-	-	-	AT91M55800A
0x10	Channel Enable Register	ADC_CHER	Write only	-	AT91M55800A
0x14	Channel Disable Register	ADC_CHDR	Write only	-	AT91M55800A
0x18	Channel Status Register	ADC_CHSR	Read only	0	AT91M55800A
0x1C	Reserved	-	-	-	AT91M55800A
0x20	Status Register	ADC_SR	Read only	0	AT91M55800A
0x24	Interrupt Enable Register	ADC_IER	Write only	-	AT91M55800A
0x28	Interrupt Disable Register	ADC_IDR	Write only	-	AT91M55800A
0x2C	Interrupt Mask Register	ADC_IMR	Read only	0	AT91M55800A
0x30	Convert Data Register 0	ADC_CDR0	Read only	0	AT91M55800A
0x34	Convert Data Register 1	ADC_CDR1	Read only	0	AT91M55800A
0x38	Convert Data Register 2	ADC_CDR2	Read only	0	AT91M55800A
0x3C	Convert Data Register 3	ADC_CDR3	Read only	0	AT91M55800A

**Digital-to-analog Converter (AT91M55800A only)**

Two identical 1-channel 10-bit digital-to-analog converters (DAC) each with a dedicated PDC channel.

**DAC Configuration/Initialization Registers**

Base Address DAC 0: 0xFFFFA8000

Base Address DAC 1: 0xFFFFAC000

**Table 17. DAC Registers**

Offset	Register	Name	Access	Reset Value	Product
0x00	Control Register	DAC_CR	Write only	-	AT91M42800A
0x04	Mode Register	DAC_MR	Read/Write	0	AT91M42800A
0x08	Data Holding Register	DAC_DHR	Read/Write	0	AT91M42800A
0x0C	Data Output Register	DAC_DOR	Read only	0	AT91M42800A
0x10	Status Register	DAC_SR	Read only	0	AT91M42800A
0x14	Interrupt Enable Register	DAC_IER	Write only	-	AT91M42800A
0x18	Interrupt Disable Register	DAC_IDR	Write only	-	AT91M42800A
0x1C	Interrupt Mask Register	DAC_IMR	Read only	0x0	AT91M42800A

**Multi-processor Interface (only available on AT91M63200)**

After a hardware reset, pins MPI\_WOE, MPI\_NLB and MPI\_NUB are not enabled by default. The user must configure the PIO controller to enable the corresponding pins for the MPI functions



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