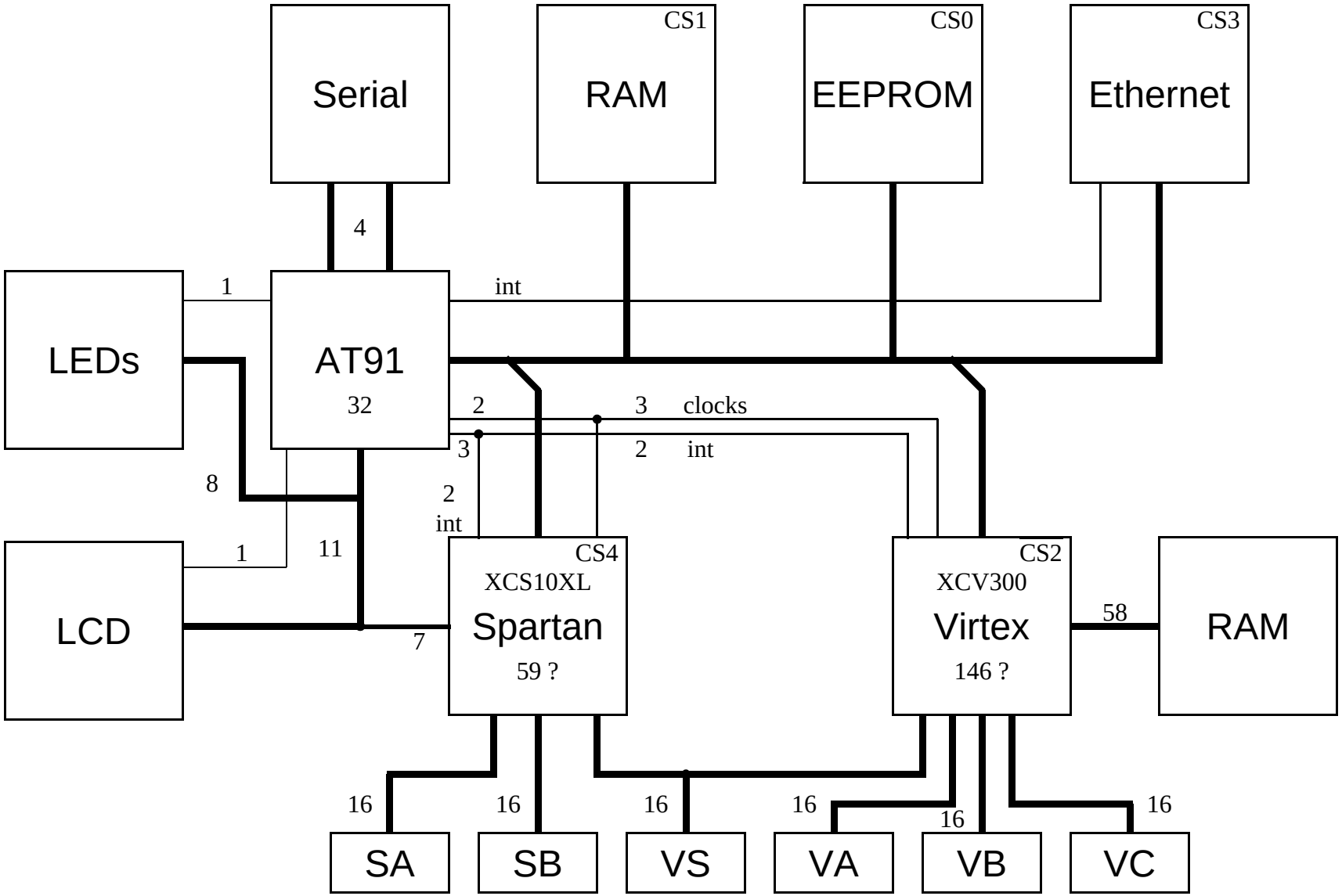

Serial
RAM
CS1
EEPROM
CS0
Ethernet
CS3
4
LEDs
1
AT91
32
int
2
3
clocks
3
2
int
8
2
int
1
11
CS4
XCS10XL
Spartan
59 ?
CS2
XCV300
Virtex
146 ?
58
RAM
LCD
7
16
16
16
16
16
16
SA
SB
VS
VA
VB
VC

AT91 Port Assignment

Port	AT91 Fn.	M.U. use	Pull	Port	AT91 Fn.	M.U. use	Pull	Port	AT91 Fn.	M.U. use	Pull	Port	AT91 Fn.	M.U. use	Pull
0		**LC_D0**		8	TIOB2	**TIM_B1**	⇑	16		**NS_PROG**	⇑	24	Boot mode	**LC_EN**	⇓
1		**LC_D1**		9	IRQ0	**S_IRQ**		17		**NV_PROG**	⇑	25	MCKO	**LC_RW**	–
2		**LC_D2**		10	IRQ1	**V_IRQ**		18		**NS_INIT**	⇑	26	NCS2	**NVIRTEX_CS**	⇑
3		**LC_D3**		11	IRQ2	**ETH_IRQ**		19		**NV_INIT**	⇑	27	NCS3	**NETH_SEL**	⇑
4		**LC_D4**	1	12	FIQ	**FIQ_B0/**[2]	⇑	20		**NLCD_BK_LT**		28	A[20]	**RAM**	–
5		**LC_D5**	1	13	SCK0	**BAUD_CLK**[3]		21	TxD1	**Spare serial**	⇑	29	A[21]	**RAM**	–
6		**LC_D6**	1	14	TxD0	**Host link**		22	RxD1	**Spare serial**		30		**LED_EN**	
7		**LC_D7**	1	15	RxD0	**Host link**		23		**LC_RS**[4]	⇑	31	CS4	**SPARTAN_CS**	⇓

[1] Large resistor pull up, smaller resistor pull down through DIP switch. Biased when floating.

[2] Also connected to ROM RDY/$\overline{\text{BUSY}}$ signal (open-drain output) and Spartan HDC – driven high at config. time

[3] Also Spartan Dout – driven low at config. time.

[4] Must be high (CS1) to programme Spartan device

Spartan XCS10XL VQ100

Pad number	Spartan Function	Name	Comments
P1	GND	GND	
P2	GCK1	SA0	
P3		SA1	
P4	TDI	NRD_NOE	Bus read enable (Used as FPGA $\overline{RD}$ after configuration.)
P5	TCK	SPARTAN_CS	Bus CS4 (Used as FPGA CS after configuration.) Driven to 0 at reset
P6	TMS	NWR0_NWE	Bus write enable #0 (Used as FPGA $\overline{WR}$ after configuration.)
P7		SA2	
P8		SA3	
P9		SA4	
P10		SA5	
P11	GND	GND	
P12	VCC	VCC	
P13		SA6	
P14		SA7	
P15		SA8	
P16		SA9	
P17		SA10	
P18		SA11	
P19		SA12	
P20		SA13	

Pad number	Spartan Function	Name	Comments
P21	GCK2	SA14	
P22	M1		Connect to ground
P23	GND	GND	
P24	M0		Connect to ground
P25	VCC	VCC	
P26	NPWRDWN		Do not connect (internal pull up)
P27	GCK3	SA15	
P28	HDC	FIQ_B0	$\overline{\text{FIQ}}$/BUS line (P12) Output at config. time
P29		SB0	
P30	LDC		Output at config. time N/C
P31		SB1	
P32		SB2	
P33		SB3	
P34		SB4	
P35		SB5	
P36	NINIT	NSPARTAN_INIT	AT91 I/O port (P18) Switch input on board Pull-up (1k-10k) required.
P37	VCC	VCC	
P38	GND	GND	
P39		SB6	
P40		SB7	
P41		SB8	
P42		SB9	

Pad number	Spartan Function	Name	Comments
P43		SB10	
P44		SB11	
P45		SB12	
P46		SB13	
P47		SB14	
P48	GCK4	SB15	
P49	GND	GND	
P50	DONE		Spartan Done (Not Connected)
P51	VCC	VCC	
P52	NPROGRAM		Drive from AT91 (P16) Internal pull-up
P53	D7	D[7]	Data bus signal
P54	GCK5	MCKI	Processor clock
P55	D6	D[6]	Data bus signal
P56		A[4]	
P57	D5	D[5]	Data bus signal
P58		A[1]	
P59		A[2]	
P60		A[3]	
P61	D4	D[4]	Data bus signal
P62		A[0]	
P63	VCC	VCC	
P64	GND	GND	

Pad number	Spartan Function	Name	Comments
P65	D3	D[3]	Data bus signal
P66		LC_D4	Biased according to set-up DIP switch
P67		LC_D5	Biased according to set-up DIP switch
P68	D2	D[2]	Data bus signal
P69		LC_D6	Biased according to set-up DIP switch
P70	D1	D[1]	Data bus signal
P71		LC_D7	Biased according to set-up DIP switch
P72	D0	D[0]	Data bus signal
P73	GCK6	BAUD_CLK	Baud clock from AT91 host serial port (P13) (also bused to Virtex.) DOUT (driven low) at Spartan config. time.
P74	CCLK	SPARTAN_CCLK	Externally derived programming clock
P75	VCC	VCC	
P76	TDO	S_IRQ	Spartan IRQ, May be used as output only – feed to AT91 interrupt input (P9)
P77	GND	GND	
P78		LC_RW	LCD RD/WR, Clock signal from AT91 at startup MCKO (P25)
P79	GCK7	TIM_B1	Programmable clock from AT91 timer TIOB2 (P8) (also bused to Virtex.)
P80	CS1	LC_RS	Pull up resistor needed. Must be high to programme device. AT91 (P23)
P81		LC_EN	AT91 (P24)
P82		VS0	
P83		VS1	
P84		VS2	
P85		VS3	

Pad number	Spartan Function	Name	Comments
P86		VS4	
P87		VS5	
P88	GND	GND	
P89	VCC	VCC	
P90		VS6	
P91		VS7	
P92		VS8	
P93		VS9	
P94		VS10	
P95		VS11	
P96		VS12	
P97		VS13	
P98		VS14	
P99	GCK8	VS15	
P100	VCC	VCC	

Virtex-E XCV300E PQ240

Pad number	Virtex Function	Name	Comments
P1	GND	GND	
P2	TMS	V_TMS	JTAG J14
P3	IO	RAM_A17	Bank 7
P4	IO	RAM_A16	Bank 7
P5	IO_VREF7	RAM_A15	Bank 7
P6	IO	RAM_A14	Bank 7
P7	IO	RAM_A13	Bank 7
P8	GND	GND	
P9	IO_VREF7	RAM_A12	Bank 7
P10	IO	RAM_A11	Bank 7
P11	IO	RAM_A10	Bank 7
P12	IO_VREF7	RAM_A9	Bank 7
P13	IO	RAM_A8	Bank 7
P14	GND	GND	
P15	VCCO	VCC1V8	Bank 7
P16	VCCINT	VCC	
P17	IO	RAM_A7	Bank 7
P18	IO	RAM_A6	Bank 7
P19	IO	RAM_A5	Bank 7
P20	IO	RAM_A4	Bank 7

Pad number	Virtex Function	Name	Comments
P21	IO	RAM_A3	Bank 7
P22	VCCINT	GND	
P23	IO_VREF7	RAM_A2	Bank 7
P24	IO	RAM_A1	Bank 7
P25	VCCO	VCC1V8	Bank 7
P26	IO	RAM_A0	Bank 7
P27	IO	RAM_D31	Bank 7
P28	IO	RAM_D30	Bank 7
P29	GND	GND	
P30	VCCO	VCC1V8	Bank 6
P31	IO	RAM_D29	Bank 6
P32	VCCINT	VCC	
P33	IO	RAM_D28	Bank 6
P34	IO	RAM_D27	Bank 6
P35	IO	RAM_D26	Bank 6
P36	IO_VREF6	RAM_D25	Bank 6
P37	GND	GND	
P38	IO	RAM_D24	Bank 6
P39	IO	RAM_D23	Bank 6
P40	IO	RAM_D22	Bank 6
P41	IO	RAM_D21	Bank 6
P42	IO	RAM_D20	Bank 6

Pad number	Virtex Function	Name	Comments
P43	VCCINT	VCC	Bank 6
P44	VCCO	VCC1V8	Bank 6
P45	GND	GND	
P46	IO	RAM_D19	Bank 6
P47	IO_VREF6	RAM_D18	Bank 6
P48	IO	RAM_D17	Bank 6
P49	IO	RAM_D16	Bank 6
P50	IO_VREF6	RAM_D15	Bank 6
P51	GND	GND	
P52	IO	RAM_D14	Bank 6
P53	IO	RAM_D13	Bank 6
P54	IO_VREF6	RAM_D12	Bank 6
P55	VCCO	VCC1V8	Bank 6
P56	IO	RAM_D11	Bank 6
P57	IO	RAM_D10	Bank 6
P58	M1	VIRTEX_M1	Connect to VCC (or GND for boundary scan mode)
P59	GND	GND	
P60	M0		Connect to GND (or VCC for boundary scan mode)
P61	VCCO	VCC1V8	Bank 5
P62	M2		Connect to GND
P63	IO	RAM_D9	Bank 5
P64	IO	RAM_D8	Bank 5

Pad number	Virtex Function	Name	Comments
P65	IO	RAM_D7	Bank 5
P66	IO_VREF5	RAM_D6	Bank 5
P67	IO	RAM_D5	Bank 5
P68	IO	RAM_D4	Bank 5
P69	GND	GND	
P70	IO_VREF5	RAM_D3	Bank 5
P71	IO	RAM_D2	Bank 5
P72	IO	RAM_D1	Bank 5
P73	IO_VREF5	RAM_D0	Bank 5
P74	IO	NRAM_B3	Bank 5
P75	GND	GND	
P76	VCCO	VCC1V8	Bank 5
P77	VCCINT	VCC	
P78	IO	NRAM_B2	Bank 5
P79	IO	NRAM_B1	Bank 5
P80	IO	NRAM_B0	Bank 5
P81	IO	NRAM_OE	Bank 5
P82	IO	NRAM_CS1	Bank 5
P83	GND	GND	Bank 5
P84	IO_VREF5	NRAM_CS0	Bank 5
P85	VCCO	VCC1V8	Bank 5
P86	IO	NRAM_WE	Bank 5

Pad number	Virtex Function	Name	Comments
P87	IO	VS0	Bank 5
P88	VCCINT	VCC	
P89	GCK1	BAUD_CLK	Bank 5 Baud clock from AT91 host serial port (P13) (also bused to Spartan.)Input only
P90	VCCO	VCC1V8	Bank 4
P91	GND	GND	
P92	GCK0	MCKI	Bank 4 Processor clockInput only Pull down resistor
P93	IO	VS1	Bank 4
P94	IO	VS2	Bank 4
P95	IO	VS3	Bank 4
P96	IO	VS4	Bank 4
P97	IO_VREF4	VS5	Bank 4
P98	GND	GND	
P99	IO	VS6	Bank 4
P100	IO	VS7	Bank 4
P101	IO	VS8	Bank 4
P102	IO	VS9	Bank 4
P103	IO	VS10	Bank 4
P104	VCCINT	VCC	
P105	VCCO	VCC1V8	Bank 4
P106	GND	GND	
P107	IO	VS11	Bank 4
P108	IO_VREF4	VS12	Bank 4

Pad number	Virtex Function	Name	Comments
P109	IO	VS13	Bank 4
P110	IO	VS14	Bank 4
P111	IO_VREF4	VS15	Bank 4
P112	GND	GND	
P113	IO	FIQ	Bank 4
P114	IO	UB	Bank 4
P115	IO_VREF4	A[6]	Bank 4
P116	VCCO	VCC1V8	Bank 4
P117	IO	A[5]	Bank 4
P118	IO	A[4]	Bank 4
P119	GND	GND	
P120	DONE		Bank 3 N/C
P121	VCCO	VCC1V8	Bank 3
P122	NPROGRAM	NVIRTEX_PROG	AT91 I/O port (P17) Pull-up resistor
P123	IO_INIT	NVIRTEX_INIT	Bank 3 AT91 I/O port (P19)Switch input on board Pull-up resistor
P124	IO_D7	D[0]	Data bus signal
P125	IO	A[3]	Bank 3
P126	IO_VREF3	A[2]	Bank 3
P127	IO	A[1]	Bank 3
P128	IO	A[0]	Bank 3
P129	GND	GND	
P130	IO_VREF3	LC_D4	Bank 3 Biased according to set-up DIP switch

Pad number	Virtex Function	Name	Comments
P131	IO	LCD5	Bank 3 Biased according to set-up DIP switch
P132	IO	LCD6	Bank 3 Biased according to set-up DIP switch
P133	IO_VREF3	LCD7	Bank 3 Biased according to set-up DIP switch
P134	IO_D6	D[1]	Bank 3 Data bus signal
P135	GND	GND	
P136	VCCO	VCC1V8	Bank 3
P137	VCCINT	VCC	
P138	IO_D5	D[2]	Bank 3 Data bus signal
P139	IO	LC_RW	Bank 3 Clock signal from AT91 at startup MCKO (P25)
P140	IO	LC_RS	Bank 3 Pull-up resistor AT91 (P23)
P141	IO	LC_EN	Bank 3 Pull-down resistor AT91 (P24)
P142	IO	VC0	Bank 3
P143	GND	GND	
P144	IO_VREF3	VC1	Bank 3
P145	IO_D4	D[3]	Bank 3 Data bus signal
P146	VCCO	VCC1V8	Bank 3
P147	IO	VC2	Bank 3
P148	VCCINT	VCC	
P149	IO	VC3	Bank 3
P150	VCCO	VCC1V8	Bank 2
P151	GND	GND	
P152	IO	VC4	Bank 2

Pad number	Virtex Function	Name	Comments
P153	IO	VC5	Bank 2
P154	IO	VC6	Bank 2
P155	IO	VC7	Bank 2
P156	IO_D3	D[4]	Bank 2 Data bus signal
P157	IO_VREF2	VC8	Bank 2
P158	GND	GND	
P159	IO	VC9	Bank 2
P160	IO	VC10	Bank 2
P161	IO	VC11	Bank 2
P162	IO	VC12	Bank 2
P163	IO_D2	D[5]	Bank 2 Data bus signal
P164	VCCINT	VCC	
P165	VCCO	VCC1V8	Bank 2
P166	GND	GND	
P167	IO_D1	D[6]	Bank 2 Data bus signal
P168	IO_VREF2	VC13	Bank 2
P169	IO	VC14	Bank 2
P170	IO	VC15	Bank 2
P171	IO_VREF2	D[8]	Bank 2
P172	GND	GND	
P173	IO	D[9]	Bank 2
P174	IO	D[10]	Bank 2

Pad number	Virtex Function	Name	Comments
P175	IO_VREF2	D[11]	Bank 2
P176	VCCO	VCC1V8	Bank 2
P177	IO_D0	D[7]	Bank 2 Data bus signal
P178	IO_DOUT_BUSY	VIRTEX_IRQ	Bank 2 Virtex Interrupt – AT91 IRQ1 (P10)
P179	CCLK	VIRTEX_CCLK	Bank 2 AT91 MCKI inverted
P180	VCCO	VCC1V8	Bank 1
P181	TDO	V_TDO	Bank 2 JTAG Header J14
P182	GND	GND	
P183	TDI	V_TDI	JTAG Header J14
P184	IO_CS	NVIRTEX_CS	Bank 1 Bus $\overline{CS2}$ Pull-up resistor
P185	IO_WRITE	NWR0_NWE	Bus write enable #0
P186	IO	D[12]	Bank 1
P187	IO_VREF1	D[13]	Bank 1
P188	IO	D[14]	Bank 1
P189	IO	D[15]	Bank 1
P190	GND	GND	
P191	IO_VREF1	VB0	Bank 1
P192	IO	VB1	Bank 1
P193	IO	VB2	Bank 1
P194	IO_VREF1	VB3	Bank 1
P195	IO	VB4	Bank 1
P196	GND	GND	

Pad number	Virtex Function	Name	Comments
P197	VCCO	VCC1V8	Bank 1
P198	VCCINT	VCC	
P199	IO	VB5	Bank 1
P200	IO	VB6	Bank 1
P201	IO	VB7	Bank 1
P202	IO	VB8	Bank 1
P203	IO	VB9	Bank 1
P204	GND	GND	
P205	IO_VREF1	VB10	Bank 1
P206	IO	VB11	Bank 1
P207	VCCO	VCC1V8	Bank 1
P208	IO	VB12	Bank 1
P209	IO	VB13	Bank 1
P210	GCK2	TIM_B1	Bank 1 Programmable clock from AT91 timer TIOB2 (P8) (also bused to Spartan.)Input only
P211	GND	GND	
P212	VCCO	VCC1V8	Bank 0
P213	GCK3	NRD_NOE	Bank 0 Bus read enable(Used as FPGA $\overline{\text{RD}}$ after configuration.) Input only
P214	VCCINT	VCC	
P215	IO	VB14	Bank 0
P216	IO	VB15	Bank 0
P217	IO	VA0	Bank 0
P218	IO_VREF0	VA1	Bank 0

Pad number	Virtex Function	Name	Comments
P219	GND	GND	
P220	IO	VA2	Bank 0
P221	IO	VA3	Bank 0
P222	IO	VA4	Bank 0
P223	IO	VA5	Bank 0
P224	IO	VA6	Bank 0
P225	VCCINT	VCC	
P226	VCCO	VCC1V8	Bank 0
P227	GND	GND	
P228	IO	VA7	Bank 0
P229	IO_VREF0	VA8	Bank 0
P230	IO	VA9	Bank 0
P231	IO_VREF0	VA10	Bank 0
P232	VCCO	VCC1V8	Bank 0
P233	GND	GND	
P234	IO	VA11	Bank 0
P235	IO	VA12	Bank 0
P236	IO_VREF0	VA13	Bank 0
P237	IO	VA14	Bank 0
P238	IO	VA15	Bank 0
P239	TCK	V_TCK	JTAG Header J14
P240	VCCO	VCC1V8	Bank 0

I/O signals

Name	AT91	Spartan	Virtex	Connector	Pulled	Function	Comments
SA[15:0]	–	various	–	SA	–	16 bits of general I/O	
SB[15:0]	–	various	–	SB	–	16 bits of general I/O	
VS[15:0]	–	various	various	SV	–	16 bits of general I/O Inter-FPGA data path	
VA[15:0]	–	–	various	VA	–	16 bits of general I/O	
VB[15:0]	–	–	various	VB	–	16 bits of general I/O	
VC[15:0]	–	–	various	VC	–	16 bits of general I/O	
RAM_A[17:0]	–	–	various	–	–	FPGA RAM address	All in bank 7
RAM_D[31:0]	–	–	various	–	–	FPGA RAM data	In banks 5 & 6
RAM_B[3:0]	–	–	P74, P78, P79, P80	–	–	FPGA RAM byte selects	In banks 5 & 7
NRAM_WE	–	–	P86	–	–	FPGA RAM write enable	
NRAM_OE	–	–	P81	–	–	FPGA RAM output enable	
NRAM_CS[1:0]	–	–	P82, P84	–	–	FPGA RAM bank selects	
LC_D[7:4]	P7-P4	P71, P69, P67, P66	P133 – P130	–	–	LCD data Processor ⇔ Spartan signals	Biased according to set-up DIP switches
LC_D[3:0]	P3-P0	–	–	–	–	LCD data	Not available to FPGA
LC_RW	P25	P78	P139	–	–	LCD direction Processor ⇔ Spartan signal	Oscilates (MCKO) after AT91 reset.
LC_RS	P23	P80	P140	–	⇑	LCD address Processor ⇔ Spartan signal	Must be high to programme Spartan (CS1)
LC_EN	P24	P81	P141	–	⇓	LCD enable Processor ⇔ Spartan signal	Also defines processor boot mode. Beware of LCD side effects.

Name	AT91	Spartan	Virtex	Connector	Pulled	Function	Comments
SPARTAN_CS	P31	P5			⇓	Spartan Chip Select after configuration	Bus CS4 (Driven low at reset)
NVIRTEX_CS	P26		P186		⇑	Virtex Chip Select after configuration	BUS NCS2
NETH_SEL	P27				⇑	Ethernet Chip Select after configura-tion	BUS NCS3
S_IRQ	P9	P76	–	–	–	Spartan interrupt Spartan ⇒ processor signal	Output only on Spartan (TDO)
V_IRQ	P10	–	P178	–	–	Virtex interrupt Virtex ⇔ processor signal	Virtex-Eoutput at config. (BUSY/ DOUT), Retained in SelectMAP
ETH_IRQ	P11	–	–	–	–	Ethernet interrupt Ethernet ⇒ processor signal	
FIQ_B0	P12	P28	P113	–	⇑	FPGA shared $\overline{\text{FIQ}}$ Processor ⇔ Spartan ⇔ Virtex bus	Spartan outputs when not programmed. Pull up allows open-drain use.
TIM_B1	P8	P79	P210	–	⇑	FPGA shared clock,(TIOB2), Processor ⇔ Spartan ⇒ Virtex bus	Input only on Virtex
BAUD_CLK	P13	P73	P89	–	–	FPGA shared clock Processor ⇔ Spartan ⇒ Virtex bus	Input only on Virtex
NSPARTAN_INIT	P18	P36	–	Button ⇒ GND	⇑	Programming control Board input switch to proc. & Spartan	Useful for (e.g.) internal reset
NVIRTEX_INIT	P19	–	P123	Button ⇒ GND	⇑	Programming control Board input switch to proc. & Virtex	Useful for (e.g.) internal reset
LED_EN	P30	–	–	DIN (as CS5)	–	Enable to ‘traffic light’ LEDs	
NLCD_BK_LT	P20	–	–	–	⇑	Enable LCD backlight	
NSPARTAN_PROG	P16	P52	–	–	⇑	Pulse low to start Spartan configuration	
NVIRTEX_PROG	P17	–	P122	–	⇑	Pulse low to start Virtex configuration	
TxD0	P14	–	–	Host serial	–		
RxD0	P15	–	–	Host serial	–		

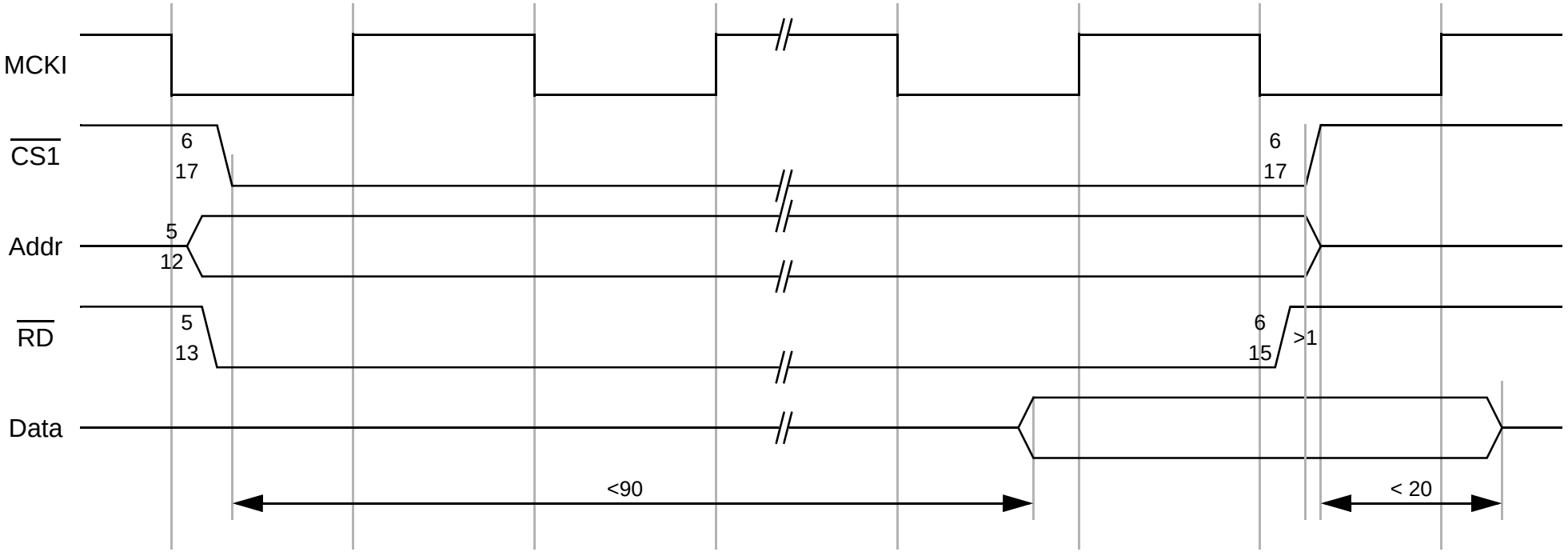
Name	AT91	Spartan	Virtex	Connector	Pulled	Function	Comments
TxD1	P21	–	–	Spare serial	⇑		Sampled at reset; tristates AT91 if low. (Also RTS0)
RxD1	P22	–	–	Spare serial	–		(Also CTS0)

Edge Connector

Pin A	Signal	Notes	Pin C	Signal	Notes
1	A[1]		1	D[0]	
2	A[2]		2	D[1]	
3	A[3]		3	D[2]	
4	A[4]		4	D[3]	
5	A[5]		5	D[4]	
6	A[6]		6	D[5]	
7	A[7]		7	D[6]	
8	A[8]		8	D[7]	
9	A[9]		9	D[8]	
10	A[10]		10	D[9]	
11	A[11]		11	D[10]	
12	A[12]		12	D[11]	
13	A[13]		13	D[12]	
14	A[14]		14	D[13]	
15	A[15]		15	D[14]	
16	A[16]		16	D[15]	
17	A[17]		17	GND	
18	A[18]		18	GND	
19	A[19]		19	A[0]/NLB	Also NLB
20	A[20]		20	NWR1_NUB	
21	A[21]		21	NWR0_NWE	

Pin A	Signal	Notes	Pin C	Signal	Notes
22	LED_EN	A[22]/CS5/P30	22	NRD_NOE	
23	NCS0	Flash select	23	NWAIT	
24	NROM_RESET	Raise to +12V to guarantee Flash writes	24	TXD1_NTRI	
25	MCKI		25	GND	
26	GND		26	NRST	
27	FIQ_B0	FLASH RDY/NBUSY	27	GND	
28	VCC		28	GND	
29	VCC		29	GND	
30	VCC		30	GND	
31	VCC		31	GND	
32	VCC		32	GND	

ROM Timing

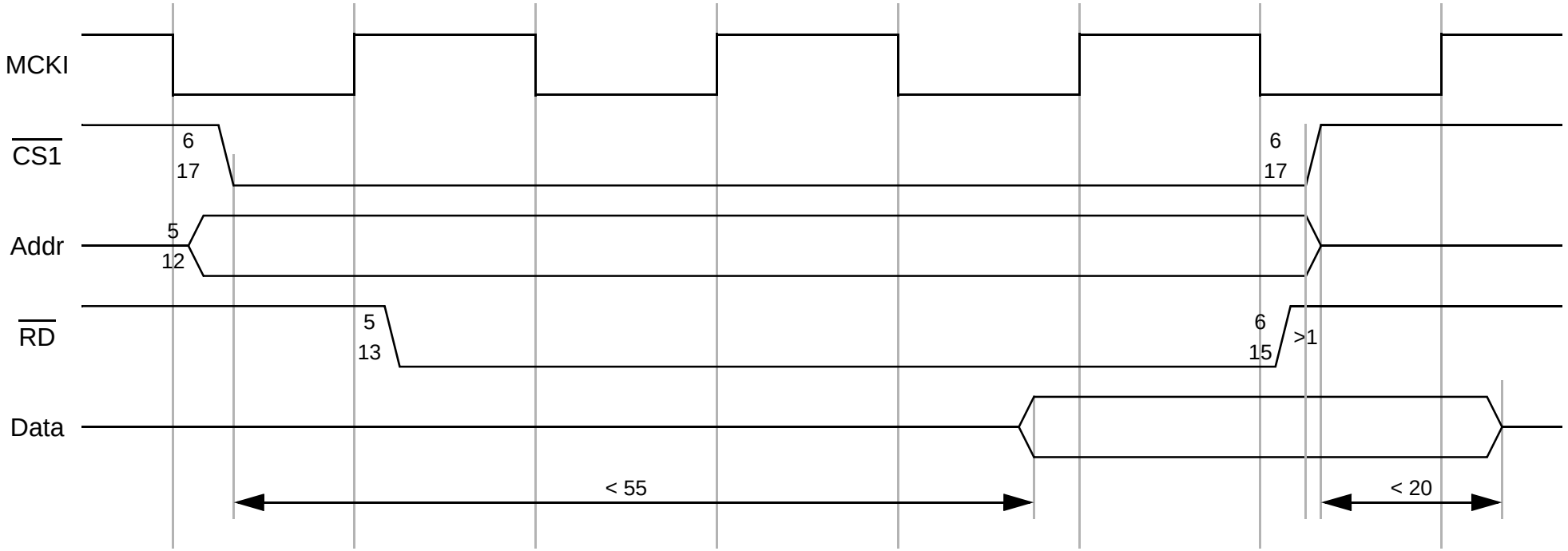


Assumes 90ns ROM
Requires three wait states plus one data float wait state for 40MHz MCKI; uses early read protocol.
Requires five wait states plus one data float wait state for 40MHz MCKI if writing.

Can reduce reads to two wait states plus one data float wait state below ~30 MHz MCKI.
Can reduce writes to four wait states plus one data float wait state below ~39 MHz MCKI.
Can reduce writes to three wait states plus one data float wait state below ~29 MHz MCKI.
No guarantee of 50ns write cycle separation provided yet!

ROM accesses are 16-bit only

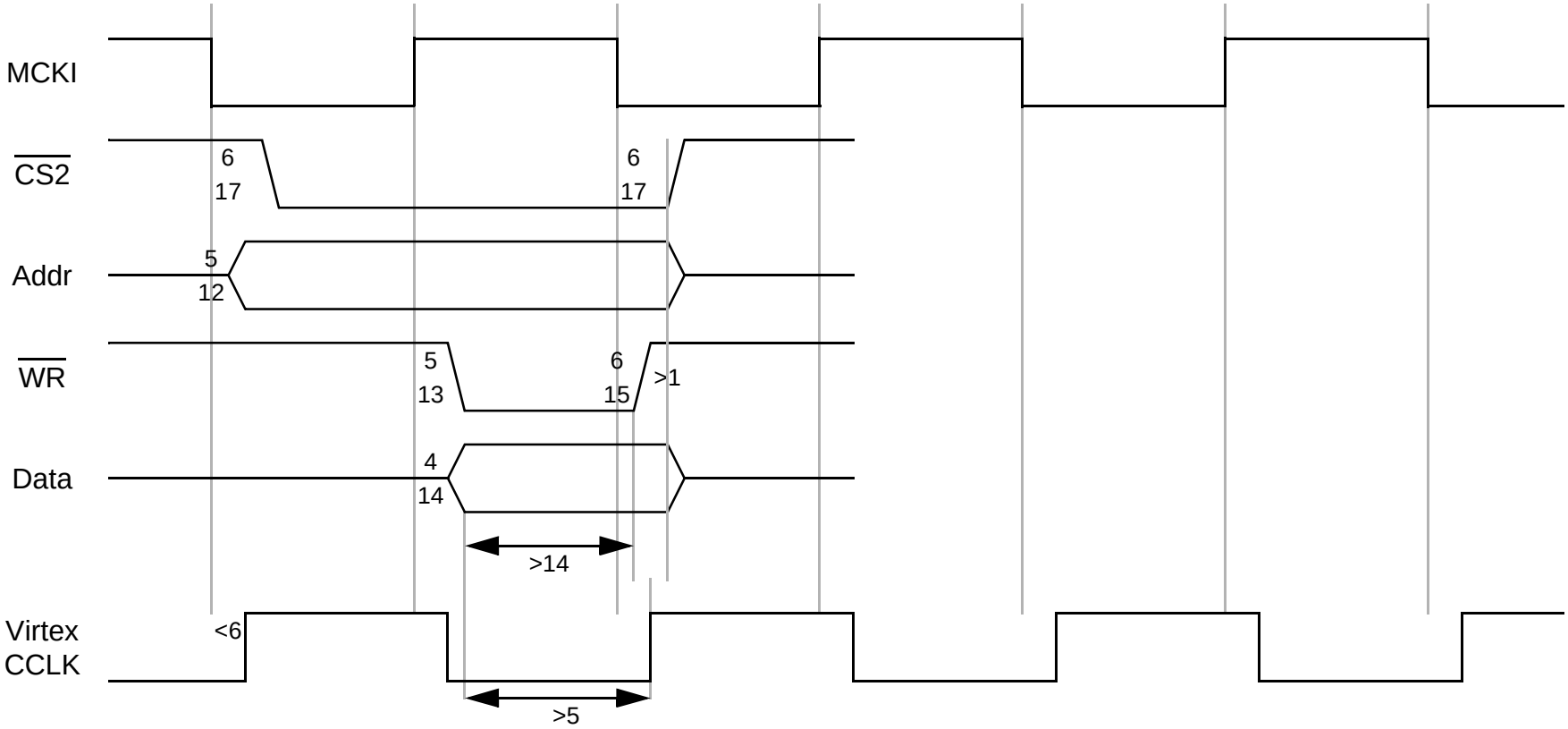
RAM Timing



Assumes 55ns RAM
Requires two wait states plus one data float wait state for 40MHz MCKI.

Can reduce to one wait state plus one data float wait state below ~25MHz MCKI.

Virtex Programming Timing

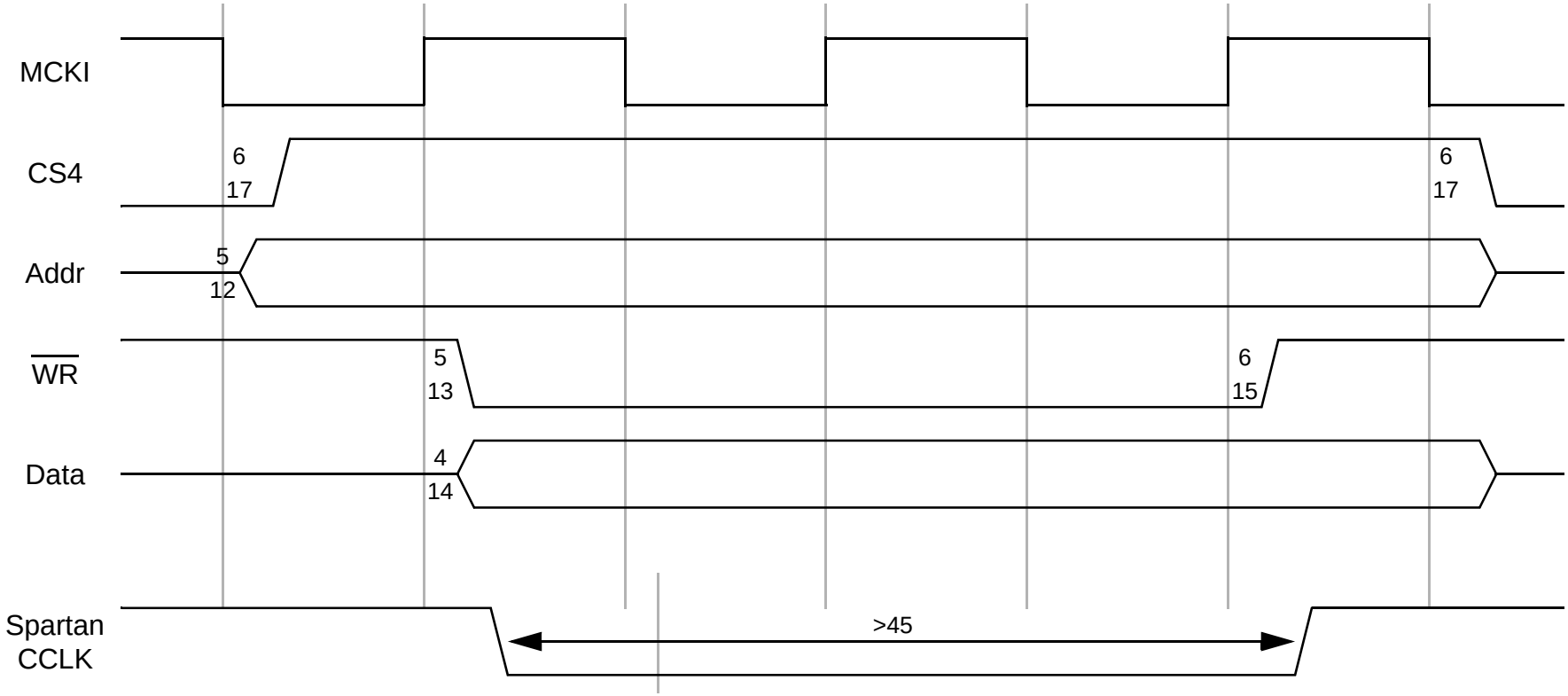


MCKI < 50MHz therefore handshaking unnecessary. Virtex_CCLK must not lag MCKI by more than 6ns.

For Virtex programming (Region 2) use 0 wait states – $\overline{CS2}$ must only be active for a single Virtex_CCLK rising edge.
Write operation will fail with more than 1 wait state because data is latched on Virtex_CCLK rising.
Interface may be reprogrammed for later FPGA operation if required.

SelectMAP Readback mode can be used with $\overline{CS2}$ asserted but $\overline{WR}$ inactive.

Spartan Programming Timing



For Spartan programming (Region 4) use 2 wait states (assuming 40MHz clock).
Readback can be performed (with ingenuity) using a different, programmed pin set under software control.

Spartan_CCLK is ($\overline{CS4}$+WR)

AT91 Pin Assignment

Pin	AT91 Fn.	ROM Pin	RAM Pin	Spartan Pin	Virtex Pin	Other	Pull	Notes
1	A0_NLB	–	LB	P62	P128	Ethernet		
2	GND	GND	GND	GND	GND	Ethernet		
3	A1	A0	A0	P58	P127	Ethernet		
4	A2	A1	A1	P59	P126	Ethernet		
5	A3	A2	A2	P60	P125	Ethernet		
6	A4	A3	A3	P56	P118	Ethernet		
7	A5	A4	A4	–	P117	Ethernet		
8	A6	A5	A5	–	P115	Ethernet		
9	A7	A6	A6	–	–	Ethernet		
10	VCC	VCC	VCC	VCC				
11	A8	A7	A7	–	–	Ethernet		
12	A9	A8	A8	–	–	Ethernet		
13	A10	A9	A9	–	–	Ethernet		
14	A11	A10	A10	–	–	Ethernet		
15	A12	A11	A11	–	–	Ethernet		
16	A13	A12	A12	–	–	Ethernet		
17	A14	A13	A13	–	–	Ethernet		
18	GND	GND	GND	GND	GND			
19	GND	GND	GND	GND	GND			

Pin	AT91 Fn.	ROM Pin	RAM Pin	Spartan Pin	Virtex Pin	Other	Pull	Notes
20	A15	A14	A14	–	–	Ethernet		
21	A16	A15	A15	–	–	Ethernet		
22	A17	A16	A16	–	–	Ethernet		
23	A18	A17	A17	–	–	Ethernet		
24	A19	A18	Decoder	–	–	Ethernet/Address Decoder U20		
25	P28_A20_CS7	A19	Decoder	–	–	Address Decoder U20		
26	P29_A21_CS6	–	Decoder	–	–	Address Decoder U20		
27	VDDCORE							VCC1V8 on AT9140008 VCC3V3 on AT9140800
28	VCC	VCC	VCC	VCC				
29	P30_A22_CS5	–	–	–	–	LED_EN		(CS5 on edge connector)
30	P31_A23_CS4	–	–	P5 (TCK)	–		⇓	Spartan CS
31	D0	D0	D0	P72 (D0)	P124 (D0)	Ethernet		
32	D1	D1	D1	P70 (D1)	P134 (D1)	Ethernet		
33	D2	D2	D2	P68 (D2)	P138 (D2)	Ethernet		
34	D3	D3	D3	P65 (D3)	P145 (D3)	Ethernet		
35	D4	D4	D4	P61 (D4)	P156 (D4)	Ethernet		
36	GND	GND	GND	GND	GND			
37	D5	D5	D5	P57 (D5)	P163 (D5)	Ethernet		
38	D6	D6	D6	P55 (D6)	P167 (D6)	Ethernet		

Pin	AT91 Fn.	ROM Pin	RAM Pin	Spartan Pin	Virtex Pin	Other	Pull	Notes
39	D7	D7	D7	P53 (D7)	P177 (D7)	Ethernet		
40	D8	D8	D8	–	P171	Ethernet		
41	D9	D9	D9	–	P173	Ethernet		
42	D10	D10	D10	–	P174	Ethernet		
43	D11	D11	D11	–	P175	Ethernet		
44	VCC	VCC	VCC	VCC				
45	D12	D12	D12	–	P186	Ethernet		
46	D13	D13	D13	–	P187	Ethernet		
47	D14	D14	D14	–	P188	Ethernet		
48	D15	D15	D15	–	P189	Ethernet		
49	P0_TCLK0	–	–	–	–	LC_D[0]	*	Weak high for short time after power on.
50	P1_TIOA0	–	–	–	–	LC_D[1]		
51	P2_TIOB0	–	–	–	–	LC_D[2]		
52	GND	GND	GND	GND	GND			
53	GND	GND	GND	GND	GND			
54	P3_TCK1	–	–	–	–	LC_D[3]		
55	P4_TIOA1	–	–	P66	P130	LC_D[4]	*	Biased according to DIP switch.
56	P5_TIOB1	–	–	P67	P131	LC_D[5]	*	Biased according to DIP switch.
57	P6_TCK2	–	–	P69	P132	LC_D[6]	*	Biased according to DIP switch.
58	P7_TIOA2	–	–	P71	P133	LC_D[7]	*	Biased according to DIP switch.

Pin	AT91 Fn.	ROM Pin	RAM Pin	Spartan Pin	Virtex Pin	Other	Pull	Notes
59	P8_TIOB2	–	–	P79 (GCLK7)	P210 (GCLK2)		⇑	Usable as clock or I/O
60	P9_IRQ0	–	–	P76 (TDO)	–			Spartan ⇒ processor only
61	VDDCORE							VCC1V8 on AT9140008 VCC3V3 on AT9140800
62	VCC	VCC	VCC	VCC				
63	P10_IRQ1	–	–	–	P178 (DOUT/BUSY)			Begins as Virtex output Can be read back
64	P11_IRQ2	–	–	–	–	Ethernet IRQ		Active high
65	GND	GND	GND	GND	GND			
66	P12_FIQ	–	–	P28 (HDC)	P113		⇑	Pull up allows open drain bus use
67	P13_SCK0	–	–	P73 (GCLK6)	89 (GCLK1)			Baud clock or bus (input only on Virtex)
68	P14_TxD0	–	–	–	–	Host Serial Buffer TX		
69	P15_RxD0	–	–	–	–	Host Serial Buffer RX		
70	P16	–	–	P52	–		⇑	Pulse low to programme Spartan
71	P17	–	–	–	P122		⇑	Pulse low to programme Virtex
72	P18	–	–	P36	–	Push button to GND	⇑	Spartan init signal
73	P19	–	–	–	P123	Push button to GND	⇑	Virtex init signal
74	P20_SCK1	–	–	–	–	LCD Backlight Power Supply	⇑	$\overline{\text{LCD Backlight}}$
75	P21_TxD1_NTRI	–	–	–	–	Spare Serial TX / Host Serial Buffer RTS0	⇑	Grounding at boot time tristates processor, With R15 & R21 fitted Serial 1 signals are RTS and CTS on Host serial (serial 0)

Pin	AT91 Fn.	ROM Pin	RAM Pin	Spartan Pin	Virtex Pin	Other	Pull	Notes
76	P22_RxD1	–	–	–	–	Spare Serial RX/ Host Serial Buffer CTS0		Grounding at boot time tristates processor, With R15 & R21 fitted Serial 1 signals are RTS and CTS on Host serial (serial 0)
77	NWR1_NUB	–	UB	–	P114	Ethernet		
78	GND	GND	GND	GND	GND			
79	NRST	–	–				⇑	Processor reset; includes button
80	NWDOVF	–	–	–	–			
81	VCC	VCC	VCC	VCC				
82	MCKI	–	–	P54 (GCLK5)	P92 (GCLK0)			
83	P23	–	–	P80 (CS1)	–	LC_RS	⇑	Must be high for Spartan configuration.
84	P24_BMS	–	–	P81	–	LC_EN	⇓	Keep low to silence LCD Low at boot time specifies 16-bit ROM
85	P25_MCK0	–	–	P78	–	LC_RW		Reflects clock at boot time
86	GND	GND	GND	GND	GND			
87	GND	GND	GND	GND	GND			
88	TMS	–	–	–	–	J15 AT91_TMS		JTAG ICE Interface
89	TDI	–	–	–	–	J15 AT91_TDI		JTAG ICE Interface
90	TDO	–	–	–	–	J15 AT91_TDO		JTAG ICE Interface
91	TCK	–	–	–	–	J15 AT91_TCk		JTAG ICE Interface
92	NRD_NOE	OE	OE	P4 (TDI)		Ethernet		
93	NWR0_NWE	WE	WE	P6 (TMS)	P185	Ethernet		

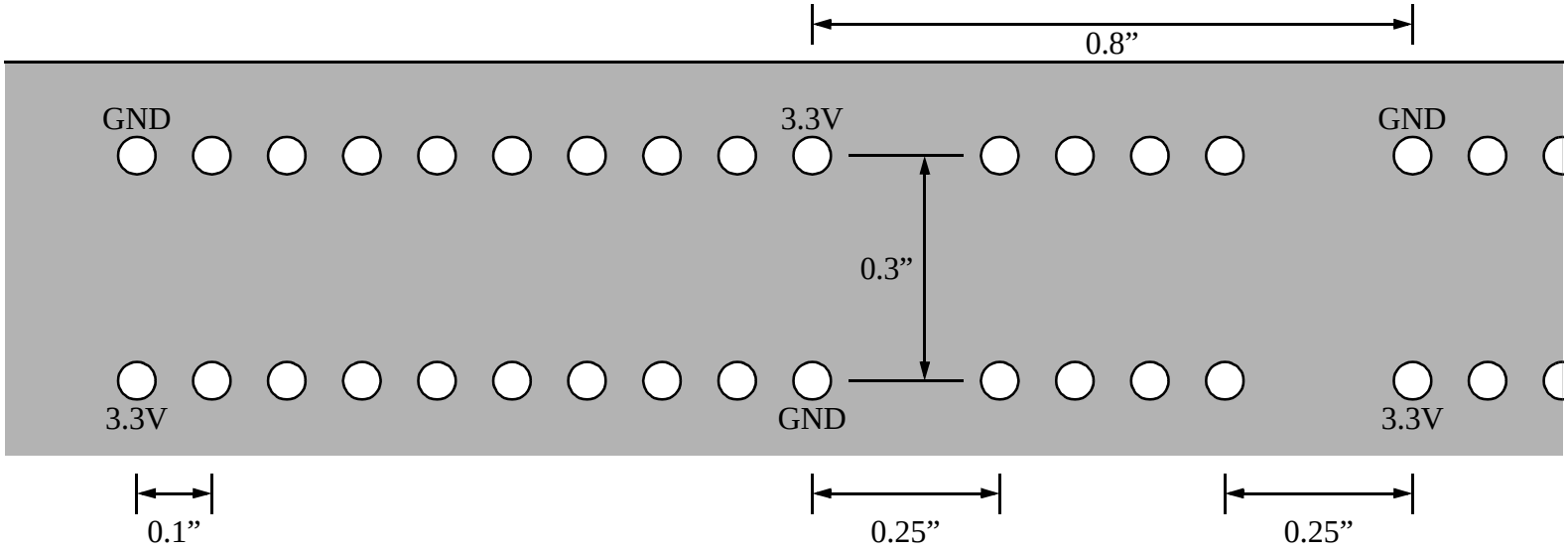
Pin	AT91 Fn.	ROM Pin	RAM Pin	Spartan Pin	Virtex Pin	Other	Pull	Notes
94	VDDCORE							VCC1V8 on AT9140008 VCC3V3 on AT9140800
95	VCC	VCC	VCC	VCC				
96	NWAIT	–	–	–	–		⇑	
97	NCS0	CE	–	–	–			Flash ROM select
98	NCS1	–		–	–	Address Decoder U20	⇑	RAM select either direct to RAM0 (via link L1) or via 3:8 decoder
99	P26_NCS2	–	–	–	184 (NVIRTEX_CS)		⇑	
100	P27_NCS3	–	–	–	–	Ethernet	⇑	

Power Supply Requirements

Name	Used for …	Nominal Voltage (V)	Min./Max. Voltage (V)	Max. current (mA)	Max. power (mW)	Quantity
	AT9140800	3.3	1.8/3.6 (4.6)	46	150 (@ 40MHz)	1
	AT9140008 I/O ring	3.3	2.7/3.6(3.6)	1.1	3.6 (@ 40MHz)	1
	AT9140008 core	1.8	1.65/1.95(1.95)	3.4	9.2 (@ 40MHz)	1
	SpartanXL	3.3	3.0/3.6 (4.0)			1
	Virtex-E I/O ring	3.3	1.2/3.6 (4.0)			1
	Virtex-E core	1.8	1.71/1.89(2)			1
	EEPROM	3.3 (5.0V Vpp optional)	3.0/3.6 (??)			1
	RAM	3.3	3.0/3.6 (3.8)	44	144	0-12
	Serial interface	3.3	3.0/5.5 (6.0)			1
	Ethernet	3.3	3.1/3.5 (6.0)	14	45	1

Edge Connector Mechanical Data

Top view



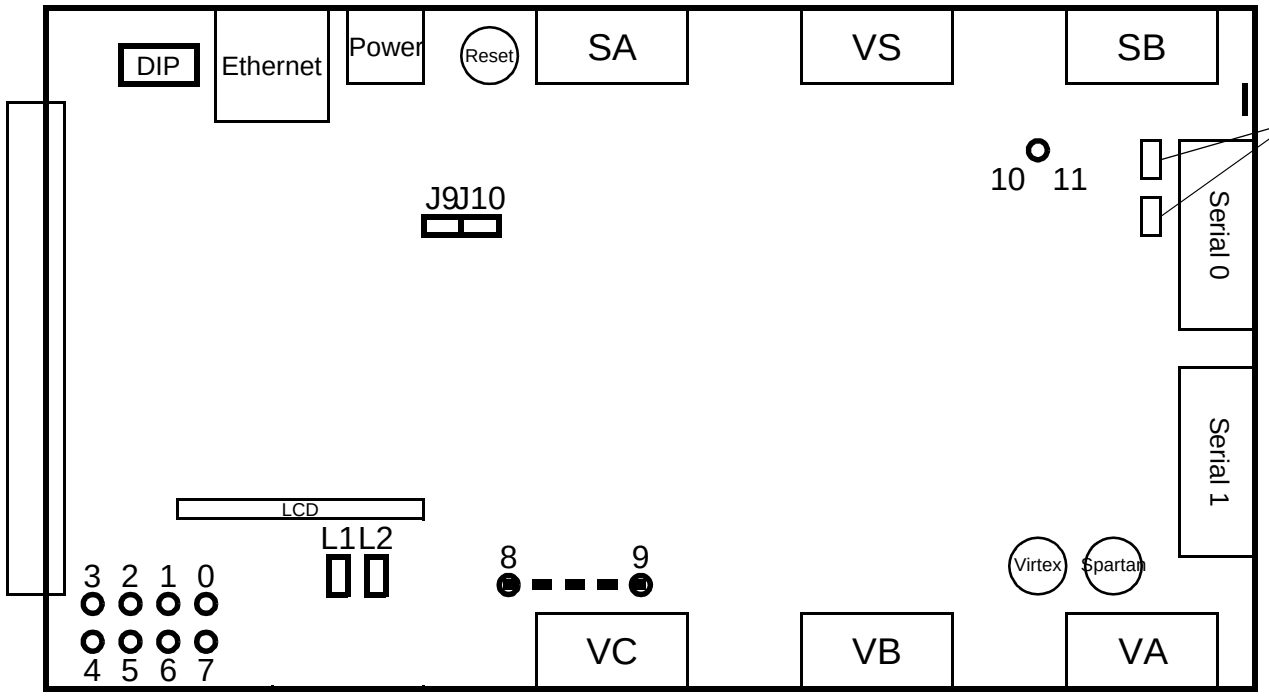
All the expansion connectors have similar pin out and are designed with rotational symmetry so that expansion boards can be inserted ‘either way up’.

The signal connectors are 20-way with options for right-angle female connectors (0.3” row pitch) or headers for ribbon cable (0.1” row pitch).

The power connectors are placed equidistantly between the signal connectors; they are offset by 0.05” to prevent false insertion.

Expansion boards may span several expansion connectors if desired.

Connectors, Links & Test Points



Fit resistors R15, R21 in order to enable Serial 1 signals as RTS/CTS on Serial 0.

- SA, SB, VS, VA, VB, and VC are all identical FPGA I/O connectors which comprise 16 I/O signals with two 3.3V and two 0V supply pins. Between them are auxiliary power connectors which reflect the input power connector.
- The four DIP switches bias the bits P7-P4 when floating on the AT91, are read in software and are intended to control the boot option.
- L1 should be fitted if the 74LCX138 is not fitted and allows a single SRAM to be used.
- L2 is normally present; if absent off-board ROM can be attached via the edge connector.
- J9 and J10 should **both** be either present or both absent. If absent the CS8900A Ethernet controller (U7) is in “memory mode” and requires an appropriately programmed EEPROM (U16); if present “IO mode” is selected and the EEPROM may be omitted.
- Test points 7-0 correspond to P7-P0 on the AT91 (P7-P4 are also accessible from the Spartan device).
- Test points 8 - 11 are ground. A wire rail may be fitted between them.