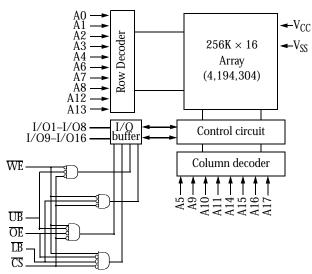


3.0V to 3.6V 256K×16 Intelliwatt[™] low-power CMOS SRAM with one chip enable

Features

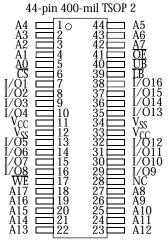
- AS6WA25616
- Intelliwatt[™] active power circuitry
- Industrial and commercial temperature ranges available
- Organization: 262,144 words \times 16 bits
- 3.0V to 3.6V at 55 ns
- Low power consumption: ACTIVE - 144 mW at 3.6V and 55 ns
- Low power consumption: STANDBY - 72 µW max at 3.6V

Logic block diagram



- 1.5V data retention
- Equal access and cycle times
- Easy memory expansion with \overline{CS} , \overline{OE} inputs
- Smallest footprint packages
 - 48-ball FBGA
 - 400-mil 44-pin TSOP 2
- ESD protection \geq 2000 volts
- Latch-up current $\geq 200 \text{ mA}$

Pin arrangement (top view)



	48-CSP Ball-Grid-Array Package								
	1	2	3	4	5	6			
А	LB	OE	A0	A1	A2	NC			
В	I/09	UB	A3	A4	CS	I/01			
С	I/010	I/011	A5	A6	I/02	I/O3			
D	V _{SS}	I/012	A17	A7	I/04	V _{CC}			
Е	V _{CC}	I/013	NC	A16	I/05	V _{SS}			
F	I/015	I/014	A14	A15	I/06	I/07			
G	I/016	NC	A12	A13	WE	I/08			
Η	NC	A8	A9	A10	A11	NC			

Selection guide

	V _{CC} Range				Power Di	ssipation
	Min	Typ ²	Max	Speed	Operating (I _{CC})	Standby (I _{SB1})
Product	(V)	(V)	(V)	(ns)	Max (mA)	Max (µA)
AS6WA25616	3.0	3.3	3.6	55	2	20

Functional description

The AS6WA25616 is a low-power CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words \times 16 bits. It is designed for memory applications where slow data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 55 ns are ideal for low-power applications. Active high and low chip selects (\overline{CS}) permit easy memory expansion with multiple-bank memory systems.

When \overline{CS} is high, or \overline{UB} and \overline{LB} are high, the device enters standby mode: the AS6WA25616 is guaranteed not to exceed 72 μ W power consumption at 3.6V and 55 ns. The device also returns data when V_{CC} is reduced to 1.5V for even lower power consumption.

A write cycle is accomplished by asserting write enable (WE) and chip select (CS) low, and UB and/or LB low. Data on the input pins I/O1–O16 is written on the rising edge of WE (write cycle 1) or CS (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (WE).

A read cycle is accomplished by asserting output enable (\overline{OE}), chip select (\overline{CS}), \overline{UB} and \overline{LB} low, with write enable (\overline{WE}) high. The chip drives I/O pins with the data word referenced by the input address. When either chip select or output enable is inactive, or write enable is active, or (\overline{UB}) and (\overline{LB}), output drivers stay in high-impedance mode.

These devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. \overline{LB} controls the lower bits, I/O1-I/O8, and \overline{UB} controls the higher bits, I/O9-I/O16.

All chip inputs and outputs are CMOS-compatible, and operation is from a single 3.0 to 3.6V supply. Device is available in the JEDEC standard 400-mm, TSOP 2, and 48-ball FBGA packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to V_{SS}		V _{tIN}	-0.5	$V_{\rm CC} + 0.5$	V
Voltage on any I/O pin relative to GND		V _{tI/O}	-0.5		V
Power dissipation		P _D	-	1.0	W
Storage temperature (plastic)		T _{stg}	-65	+150	°C
Temperature with V _{CC} applied		T _{bias}	-55	+125	°C
DC output current (low)		I _{OUT}	-	20	mA

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

CS	WE	ŌĔ	LB	UB	Supply Current	I/01–I/08	I/O9–I/O16	Mode
Н	Х	Х	Х	Х	I _{SB}	High Z	High Z	Standby (I _{SB})
L	Х	Х	Н	Н	1SB		Ingn Z	Standby (ISB)
L	Н	Н	Х	Х	I _{CC}	High Z	High Z	Output disable (I_{CC})
			L	Н		D _{OUT}	High Z	
L	Н	L	Н	L	I _{CC}	High Z	D _{OUT}	Read (I _{CC})
			L	L		D _{OUT}	D _{OUT}	
			L	Н		D _{IN}	High Z	
L	L	Х	Н	L	I _{CC}	High Z	D _{IN}	Write (I _{CC})
			L	L		D _{IN}	D _{IN}	

Key: X = Don't care, L = Low, H = High.



(over the operating condition (over the operating range)									
Parameter	Description	Test	Conditions	Min	Max	Unit			
V _{OH}	Output HIGH Voltage	$I_{OH} = -2.1 mA$	$V_{CC} = 3.0 - 3.6V$	2.4		V			
V _{OL}	Output LOW Voltage	$I_{OL} = 2.1 \text{mA}$	$V_{CC} = 3.0 - 3.6V$		0.4	V			
V _{IH}	Input HIGH Voltage		$V_{CC} = 3.0 - 3.6V$	2.2	$V_{CC} + 0.5$	V			
V _{IL}	Input LOW Voltage		$V_{CC} = 3.0 - 3.6V$	-0.5	0.8	V			
I _{IX}	Input Load Current	GND	$\leq V_{IN} \leq V_{CC}$	-1	+1	μA			
I _{OZ}	Output Load Current	$GND \le V_0 \le V_0$	V _{CC;} Outputs High Z	-1	+1	μΑ			
I _{CC}	V _{CC} Operating Supply Current	$\label{eq:cs} \begin{split} \overline{\text{CS}} &= V_{IL}, V_{IN} = V_{IL} \\ \text{or } V_{IH}, I_{OUT} = 0 \\ f &= 0 \end{split}$	$V_{CC} = 3.6V$		2	mA			
I _{CC1} @ 1 MHz	Average V _{CC} Operating Supply Current at 1 MHz	$\label{eq:cs_star} \begin{array}{l} \overline{\text{CS}} \leq 0.2\text{V}, \text{V}_{IN} \leq 0.2\text{V} \\ \text{or} \text{V}_{IN} \geq \text{V}_{CC} - 0.2\text{V}, \\ f = 1 \text{mS} \end{array}$	$V_{CC} = 3.6V$		5	mA			
I _{CC2}	Average V _{CC} Operating Supply Current	$\label{eq:VIL} \begin{split} \overline{\text{CS}} \neq \text{V}_{\text{IL}}, \ \text{V}_{\text{IN}} = \text{V}_{\text{IL}} \text{ or } \\ \text{V}_{\text{IH}}, \ \text{f} = \text{f}_{\text{Max}} \end{split}$	$V_{CC} = 3.6V$		40	mA			
I _{SB}	CS Power Down Current; TTL Inputs		$V_{CC} = 3.6V$		100	μΑ			
I _{SB1}	CS Power Down Current; CMOS Inputs	$\label{eq:cs} \begin{split} \overline{\text{CS}} &\geq \text{V}_{\text{CC}} - 0.2 \text{V or} \\ \overline{\text{UB}} &= \overline{\text{LB}} \geq \text{V}_{\text{CC}} - 0.2 \text{V}, \\ \text{other inputs} &= 0 \text{V} - \text{V}_{\text{CC}}, \\ f &= 0 \end{split}$	$V_{CC} = 3.6V$		20	μΑ			

Recommended operating condition (over the operating range)

Capacitance (f = 1 MHz, T_a = Room temperature, V_{CC} = NOMINAL)²

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, CS, WE, OE, LB, UB	$V_{IN} = 0V$	5	pF
I/O capacitance	C _{I/O}	I/O	$V_{\rm IN} = V_{\rm OUT} = 0V$	7	pF

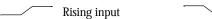


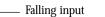
Read cycle (over the operating range)^{3,9}

Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	-	ns	
Address access time	t _{AA}	-	55	ns	3
Chip select (\overline{CS}) access time	t _{ACS}	-	55	ns	3
Output enable (OE) access time	t _{OE}	_	25	ns	
Output hold from address change	t _{OH}	10	-	ns	5
CS low to output in low Z	t _{CLZ}	10	_	ns	4, 5
CS high to output in high Z	t _{CHZ}	0	20	ns	4, 5
OE low to output in low Z	t _{OLZ}	5	_	ns	4, 5
UB/LB access time	t _{BA}	-	55	ns	
UB/LB low to low Z	t _{BLZ}	10	-	ns	4, 5
<u>UB/LB</u> high to high Z	t _{BHZ}	0	20	ns	4, 5
OE high to output in high Z	t _{OHZ}	0	20	ns	4, 5
Power up time	t _{PU}	0	_	ns	4, 5
Power down time	t _{PD}	-	55	ns	4, 5

Shaded areas indicate preliminary information.

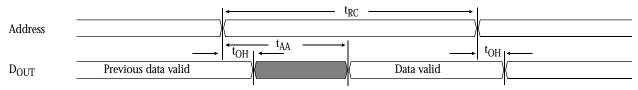
Key to switching waveforms



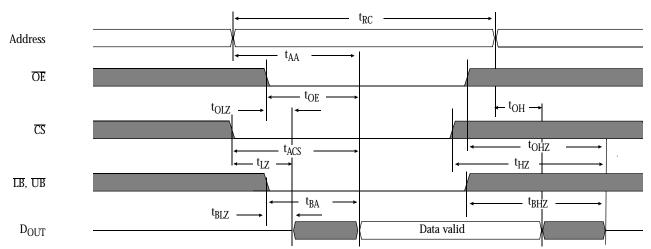


Undefined/don't care

Read waveform 1 (address controlled)^{3,6,7,9}



Read waveform 2 (CS, OE, UB, LB controlled)^{3,6,8,9}

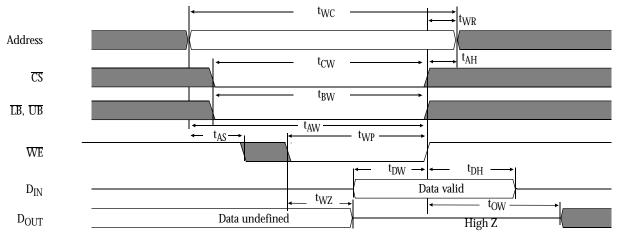




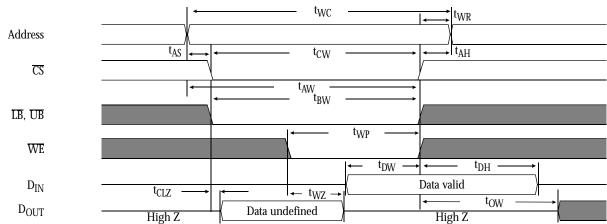
Write cycle (over the operating range)¹¹.

Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	-	ns	
Chip select to write end	t _{CW}	40	-	ns	12
Address setup to write end	t _{AW}	40	-	ns	
Address setup time	t _{AS}	0	-	ns	12
Write pulse width	t _{WP}	35	-	ns	
Write recovery time	t _{WR}	0	-	ns	
Address hold from end of write	t _{AH}	0	-	ns	
Data valid to write end	t _{DW}	25	-	ns	
Data hold time	t _{DH}	0	-	ns	4, 5
Write enable to output in high Z	t _{WZ}	0	20	ns	4, 5
Output active from write end	t _{OW}	5	-	ns	4, 5
UB/LB low to end of write	t _{BW}	35	-	ns	

Write waveform 1 (WE controlled)^{10,11}



Write waveform 2 (CS controlled)^{10,11}



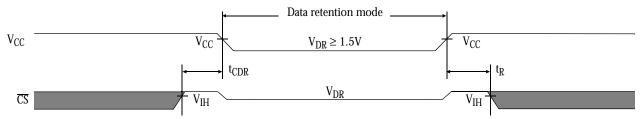
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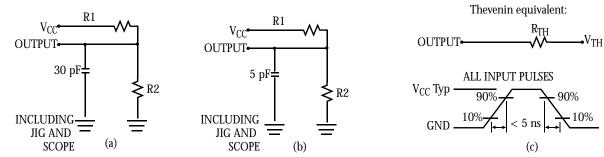
Data retention characteristics (over the operating range)^{13,5}

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V _{DR}	$V_{\rm CC} = 1.5 V$	1.5V	-	V
Data retention current	I _{CCDR}	$\overline{\text{CS}} \ge \text{V}_{\text{CC}} - 0.1\text{V or}$ $\overline{\text{UB}} = \overline{\text{LB}} = > \text{V}_{\text{CC}} - 0.1\text{V}$	_	10	μA
Chip deselect to data retention time	t _{CDR}	$V_{\rm IN} \ge V_{\rm CC} - 0.1 V$ or	0	-	ns
Operation recovery time	t _R	$V_{\rm IN} \le 0.1 \rm V$	t _{RC}	-	ns

Data retention waveform



AC test loads and waveforms



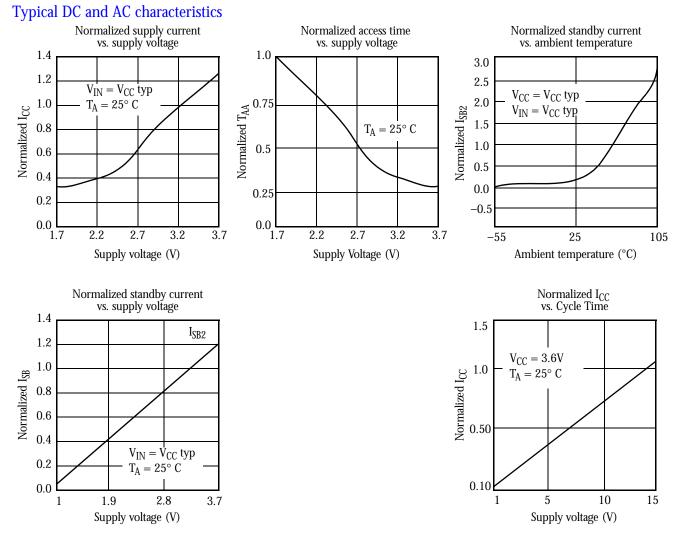
Parameters	$V_{CC} = 3.6V$	Unit
R1	1523	Ohms
R2	1142	Ohms
R _{TH}	476	Ohms
V _{TH}	1.4V	Volts

Notes

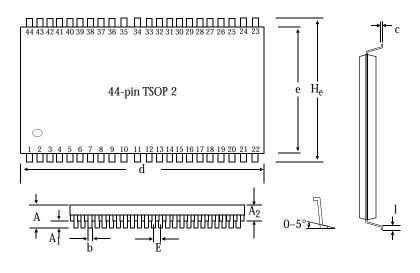
- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{\text{CS}}$ is required to meet I_{SB} specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see AC Test Conditions.
- 4 t_{CLZ} and t_{CHZ} are specified with $C_L = 5pF$ as in Figure C. Transition is measured ± 500 mV from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- 6 WE is HIGH for read cycle.
- 7 $\overline{\text{CS}}$ and $\overline{\text{OE}}$ are LOW for read cycle.
- 8 Address valid prior to or coincident with \overline{CS} transition LOW.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 CS or WE must be HIGH during address transitions. Either CS or WE asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 N/A.
- 13 1.5V data retention applies to commercial and industrial temperature range operations.
- 14 C = 30pF, except at high Z and low Z parameters, where C = 5pF.

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Package diagrams and dimensions

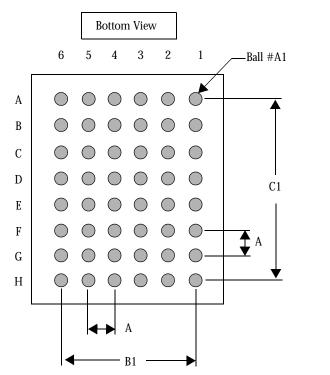


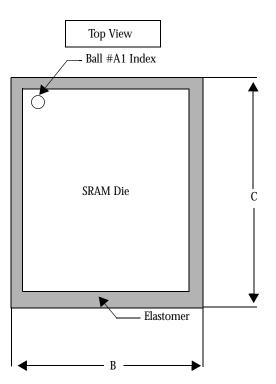
	44-pin TSOP 2			
	Min	Max		
	(mm)	(mm)		
А		1.2		
A_1	0.05			
A_2	0.95	1.05		
b	0.25	0.45		
С	0.15 (t	ypical)		
d	18.28	18.54		
e	10.06	10.26		
H _e	11.56	11.96		
Е	0.80 (typical)			
1	0.40	0.60		

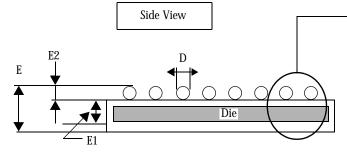
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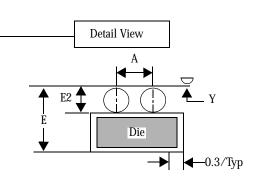


48-ball FBGA









	Minimum	Typical	Maximum
А	-	0.75	-
В	6.90	7.00	7.10
B1	-	3.75	-
С	10.90	11	11.10
C1	_	5.25	-
D	0.30	0.35	0.40
Е	-	_	1.20
E1	-	0.68	-
E2	0.22	0.25	0.27
Y	-	_	0.08

Notes

- 1. Bump counts: 48 (8 row \times 6 column).
- 2. Pitch: $(x,y) = 0.75 \text{ mm} \times 0.75 \text{ mm}$ (typ).
- 3. Units: millimeters.
- 4. All tolerance are ± 0.050 unless otherwise specified.
- 5. Typ: typical.
- 6. Y is coplanarity: 0.08 (max).



Ordering codes

Speed (ns)	Ordering Code	Package Type	Operating Range	
55	AS6WA25616-TC	44-pin TSOP 2	- Commercial	
55	AS6WA25616-BC	48-ball fine pitch BGA		
55	AS6WA25616-TI	44-pin TSOP 2	Industrial	
55	AS6WA25616-BI	48-ball fine pitch BGA		

Part numbering system

U			
AS6WA	25616	Т, В	C, I
SRAM Intelliwatt™ prefix	Device number	Package: T: TSOP 2 B: CSP/BGA	Temperature range: C: Commercial: 0° C to 70° C I: Industrial: -40° C to 85° C

7/9/02; v.1.3

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